4H-SiC METAL OXIDE SEMICONDUCTOR DEVICES

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ABSTRACT

Metal oxide semiconductor (MOS) devices are the most important component in advanced integrated circuits (ICs). The success of Si in CMOS technology is owing to the excellent interface formed between Si and SiO_2. However, Si-based electronic devices are not suitable to operate in high power, high frequency and high temperature conditions due to material limitations. 4H-SiC with a wide bandgap, high critical electric field, high thermal conductivity and high saturation drift velocity, is an attractive semiconductor material for extreme conditions. However, high quality oxide-semiconductor interfaces are still a major challenge in 4H-SiC MOS devices. This thesis focuses on interface studies of 4H-SiC MOS devices. The main aim is to produce high quality oxide/4H-SiC interfaces by the introduction of an ultrathin SiO_2 layer between deposited oxides and 4H-SiC.

Ultrathin SiO_2 layers can be grown on 4H-SiC using a low thermal budget technique followed by Al_2O_3 deposition using ALD. N-type and p-type MOS capacitors were fabricated using a gate oxidation of 600 °C for 3 min, which produced SiO_2 of thickness 0.7 nm as estimated using ARXPS. Electrical characterisation demonstrates an interface trap density (D_{it}) of 4-6 × 10^{11} $cm^{-2}eV^{-1}$ at 0.2 eV from the conduction and valence band edges. This represents a reduction in D_{it} by 1-2 orders of magnitude compared to the devices fabricated at 1150 °C for 180 min in the furnace. Furthermore, field effect channel mobility as high as 125 $cm^2/V.s$ and a subthreshold slope of 130 mV/dec were obtained from MOSFETs using similar gate stacks. The mobility of MOSFETs decreases with increasing temperature indicating that the electron conductivity is limited by phonon scattering rather than Coulomb scattering, and proves that D_{it} at the oxide/4H-SiC has been reduced. The ultrathin layer is believed to be a good interface layer between Al_2O_3 and 4H-SiC. As the temperature and time of the oxidation process increased, resulting in thicker SiO_2, the values of D_{it} increased for both p-type and n-type MOS capacitors.

Ultrathin SiO_2 layers were also grown underneath a deposited SiO_2 layer by N_2O annealing at 1175 °C. From n-type MOS capacitor results, the lowest values of D_{it} obtained were 1.7 × 10^{12} $cm^{-2}eV^{-1}$ at 0.2 eV below the conduction band edge, for gate oxides consisting of 60 nm deposited SiO_2 followed by 90 min of N_2O annealing. This process produced a SiO_2 layer 0.68 nm thick, estimated using the Deal-Grove model. The values of D_{it} increased as the grown SiO_2 thicknesses became thicker or thinner than 0.68 nm. This trend is similar to what

was found in ultrathin SiO_2/Al_2O_3 gate stacks of MOS capacitors proving that 0.7 nm thick is the best thickness of SiO_2 to use for 4H-SiC MOS devices.

Electrical measurement up to 300 °C proved that these fabricated MOS devices are able to operate well at high temperature. MOSFETs utilizing ultrathin SiO_2/Al_2O_3 gate stacks could retain their enhancement mode behaviour even at high temperature demonstrating the devices capability to be operated in extreme conditions. Both gate stacks also exhibited a low leakage current and were able to withstand electric fields far above 3 MV/cm, which is needed for actual operating system.

The scope of these findings points to solutions for the interface challenges in 4H-SiC MOS devices. A thermally grown SiO_2 layer 0.7 nm thick exhibited the lowest D_{it} values for both gate stacks and also produced high field effect channel mobility in MOSFETs. It is anticipated that this fabrication approach will mitigate the oxide/4H-SiC interface problem and contribute towards the development of improved power electronic devices.

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Publications

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Abbreviations

AC – Alternating Current
AFM – Atomic Force Microscopy
ALD – Atomic Layer Deposition
ARXPS – Angle Resolved X-Ray Photoelectron Spectroscopy
BOE – Buffered Oxide Etch
CMOS– Complementary Metal Oxide Semiconductor
C-V – Capacitance-Voltage
DC– Direct Current
DLTS– Deep Level Transient Spectroscopy
EELS – Electron Energy Loss Spectroscopy
FET – Field Effect Transistor
GND – Ground/Earth
G-V – Conductance-Voltage
HRTEM– High Resolution Transmission Electron Microscopy
IMFP– Inelastic Mean Free Path
IPA – Isopropyl Alcohol
I-V– Current-Voltage
MOS – Metal Oxide Semiconductor
MOSFET – Metal Oxide Semiconductor Field Effect Transistor
MS – Metal Semiconductor
NMP – N-Methyl-2-pyrrolidone
PECVD – Plasma Enhanced Chemical Vapour Deposition
PVD – Physical Vapour Deposition
RCA – Radio Company of America
RF – Radio Frequency
RIE – Reactive Ion Etching
RMS – Root Mean Square
RTP – Rapid Thermal Processing
SCM – Scanning Capacitance Microscopy
SIMS– Scanning Ion Mass Spectrometry
TMA – Trimethylaluminium
TRIM – Transport of Ions in Matter
XPS – X-Ray Photoelectron Spectroscopy

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Chapter 1

Introduction

1.1

The evolution of semiconductor materials and devices has been driving many innovations in modern society. The revolution began in 1947-1948 with the establishment of the germanium (Ge)-based bipolar transistor [1, 2] and silicon (Si)-based metal oxide semiconductor field effect transistors (MOSFETs) in 1959 [3]. Since then, with continuous effort, there have been a lot of new inventions and improvements in semiconductor technology. Nowadays, it is widely known that modern society is very dependent on electrical appliances, and hence semiconductor-based technology is extremely important. In term of energy efficiency, many advances have been achieved by Si-based power devices, but these have reached their theoretical physical limits and thus it is difficult to achieve any further breakthroughs [4, 5]. The major applications of power devices, include power transmission, electric traction, motor control, robotics, electric/hybrid cars, switching power supply system, and domestic appliances.

From the most recent report in 2014, global electrical energy consumption represented 21% of total energy consumption [6] and this trend is expected to rise in the future. However, 10% of electric power is lost as heat during power conversion and only power conversion efficiency up to 85-95% can be obtained using current technology [7]. Therefore, electric power dissipation during power conversion is still a major problem which needs to be addressed. Typically, electric power conversion is used to convert and regulate electric power in the form of frequency conversion (AC-AC) and voltage conversion (AC-DC, DC-AC, DC-DC) [8]. To

obtain higher device efficiency, wide bandgap semiconductor materials are an alternative, as they are suitable for operation in high-power, high-frequency and high-temperature conditions.

Silicon carbide (SiC) is one of the most promising alternatives to replace Si in power electronic devices. As a wide bandgap semiconductor, it offers huge advantages for operation at higher frequencies, voltages and temperatures. Wide bandgap materials are typically defined as having a bandgap over 2 eV [9]. The bandgap of SiC depends on its polytype structures, 3C-SiC = 2.36 eV, 6H-SiC = 3.02 eV and 4H-SiC = 3.26 eV. These values are significantly higher than those of commonly used semiconductors such as Si and Gallium Arsenide (GaAs) with bandgaps of 1.12 eV and 1.42 eV respectively [7, 10-12].

In terms of the critical electric field, SiC and particularly 4H-SiC displays a high breakdown voltage which can withstand up to approximately 2.8 MV/cm before material collapse and functional failure [7]. This value is far better than that of Si, which can only resist 0.3 MV/cm or only 10% of 4H-SiC's capability. Such superior properties have enabled 4H-SiC devices to be operational at very high power levels and high voltages, for instance in power transistors, diodes and power thyristors as well as power microwave devices. In addition, heat transfer or thermal conductivity (λ) according to Fourier's Law across 4H-SiC material is nearly 3.3 W/cm.K [7]. This high value is necessary in power electronic devices in order to dissipate heat efficiently into the environment and to sustain operation at very high ambient temperatures. On the other hand, Si and GaAs show comparatively poor heat transfer rates with Si = 1.3 W/cm.K and GaAs = 0.5 W/cm.K [12]. These materials might be good for room temperature operation but not in extreme conditions. However, 4H-SiC shows less bulk electron mobility (1200 cm^2/Vs parallel to C-face) compared to Si 1450 (cm^2/Vs) and GaAs (9200 cm^2/Vs) at room temperature respectively [12].

An advantage of SiC material in comparison with other wide bandgap semiconductors is that it can produce native oxide from its bulk via the oxidation process which is similar to Si. SiC also exhibits superior physical properties in term of its high critical electric field, better thermal conductivity, high melting point and large electron saturation velocity. Those considerable merits exist regardless of the polytype structure of SiC, and hence it is a promising semiconductor material for high-frequency, high-power and high-temperature application. Table 1.1 summarises the material properties of candidate semiconductors for power electrical devices [7, 10-13].

Material	Bandgap E_g (eV)	Breakdown field E_c (MV/cm)	Thermal conductivity λ (W/cm.K)	Electron mobility μ (cm^2/Vs)	Relative dielectric constant ε_r
Si	1.12	0.3	1.3	1450	11.9
GaAs	1.42	0.4	0.5	9200	12.4
4H-SiC	3.26	2.8	3.3	1200	9.66

Table 1.1: Physical properties of semiconductor materials [7].

1.2 Research Objective

The aim of this research is to reduce the density of interface traps (D_{it}), which are believed to be the main source of reductions in electron mobility in 4H-SiC MOSFETs. The D_{it} are believed to originate from C defects that are generated by thermal oxidation. By growing an ultrathin SiO_2 layer between the deposited dielectric and 4H-SiC substrate, the generation of C defects can be minimised and thus the electron mobility in the channel will be enhanced. The specific objectives of the study are as follows:

1. To grow an ultrathin SiO_2 layer as a good interface layer on 4H-SiC using a low thermal budget technique, together with a deposited Al_2O_3 layer.
2. To grow an ultrathin SiO_2 layer as a good interface layer underneath deposited SiO_2 via post-oxidation annealing (POA) in N_20 ambient.
3. To optimize oxide layer thickness, oxidation parameter conditions and dielectric parameters in order to produce a fully optimized MOS capacitor.
4. To fabricate 4H-SiC MOSFETs with high electron mobility using a low thermal budget technique.
5. To characterize the electrical and physical properties of the devices using I-V, C-V, ARXPS and AFM measurements.
6. To study the stability of MOS devices at high temperatures.
7. To investigate the cause of limited channel mobility, and to examine the relationship between electron mobility and D_{it}.

1.3 Thesis Outline

The novelty and challenge of this research arise from its aim to reduce the concentration of D_{it} originating from the formation of C defects by thermal oxidation, and to thus increase electron mobility in MOSFETs. A number of other research groups have demonstrated high electron

mobility in 4H-SiC MOSFETs, but the factors limiting mobility are not fully understood and the stability of such devices remains an issue.

Chapter 2

Chapter 2 begins with a background study of the properties of SiC and the challenges in developing a high quality interface between the dielectric and the SiC substrate. Then, previously reported work concerning the development of MOS interface technology is reviewed. Finally, reports of the relationship between electron mobility and D_{it} in devices are described and discussed.

Chapter 3

In this chapter, the fundamental principles of MOS devices are discussed, including ideal and non-ideal MOS capacitors. Next, the electrical characterisation techniques that are used in this thesis are considered. The model of D_{it} and factors limiting electron mobility is carefully explained. Furthermore, the main types of physical characterisation used to estimate the thickness of the grown ultrathin SiO_2 layer and deposited Al_2O_3 and SiO_2 layers are explained. Lastly, the main fabrication processes, including sample preparation, optical lithography, oxidation and metallisation, are described.

Chapter 4

The fabrication of MOS capacitors using a low thermal budget technique is demonstrated in chapter 4. The metal semiconductor (MS) contact which connects the device to the outer circuitry is optimised and the best possible process is used for the fabrication of complete MOS capacitors. Then, the electrical characterisation of p-type and n-type MOS capacitors to obtain the lowest values of D_{it} is discussed. In addition the stability of the devices during high temperature measurements and the robustness of the gate dielectric are described.

Chapter 5

After achieving the lowest values of D_{it} in the MOS capacitors using a low thermal budget technique as outlined in chapter 4, the next step is to develop MOSFETs using similar gate stack formation parameters. Prior to the fabrication of the MOSFETs, the carbon cap removal process, which also uses a low thermal budget technique, is optimised. Then, the electrical characterisation of the MOSFETs used to demonstrate electron mobility and current carrying capability is discussed. High temperature measurements up to 300 °C were performed to observe the stability of the MOSFETs.

Chapter 6

In this chapter, the gate dielectric of MOS capacitors was fabricated by growing an ultrathin SiO_2 layer underneath deposited SiO_2 via POA in N_2O ambient at 1175 °C. The thickness of the deposited SiO_2 and POA time were varied in order to achieve the lowest possible value of D_{it}. The stability of the MOS capacitors at high temperature is also demonstrated. At the end of this chapter, the current conduction mechanism in the gate dielectric is discussed.

Finally, the summary and conclusions of this thesis are presented in chapter 7.

Chapter 2

Background

2.1 Introduction

Silicon Carbide (SiC) material contains Silicon (Si) and carbon (C) atoms and was first discovered by Berzelius in 1824 [14] when it was described as a rare earth natural material. Then a process of the synthesis of SiC from silica, C and some additives was discovered by Edward Acheson, an American chemist, in 1892 [15]. He had worked with Thomas Edison in successfully making a conducting carbon that Edison could use in his legendary invention of electric light bulbs.

Half a century later, in 1955, Jan Lely from Philips company in Eindhoven, Netherlands developed a method to grow relatively pure SiC by a sublimation technique named the Lely method [16]. Since then, it has become an attractive material due to its relatively high crystal quality which is compatible for use in the semiconductor device industry. At the beginning of the 1990s, Cree dominated SiC device production and in 2014 it announced annual revenue up to 1.65 billion dollars [17]. Huge attention to SiC development has also been attributed to a new gigantic hub for SiC research worth 200 million dollars which was announced by the President of United States in January 2014. In September 2015 Cree rebranded its power and radio frequency division as Wolfspeed in order to further focus on SiC development.

2.1.1 Physical and electrical properties

SiC is a compound semiconductor which consists of 50% Si and 50% C. Both Si and C atoms are tetravalent elements and have four valence electrons in their outermost shells. Si and C atoms are tetrahedrally bonded with covalent bonds by sharing electron pairs in the sp^3-hybrid orbital with a strong bond energy of 4.6 eV to form a SiC crystal [7].

From a crystallographic perspective, SiC is identified as exhibiting polytypism [7, 18, 19], where the material can exist in different crystal structures without changes in chemical composition. Commonly, each material can only have one stable structure, often either a zincblend or wurtzite structure. Surprisingly, SiC has more than 200 polytype structures. In SiC, polytypes are distinguished by the Si-C bilayers number in the unit cell and the crystal system (C for cubic. H for hexagonal and R for rhombohedral). The most commonly used SiC polytypes are 3C-SiC, 4H-SiC and 6H-SiC, as illustrated in Figure 2.1 where open and closed circles represent Si and C atoms respectively. In this close-packed structure, A, B and C are potentially occupied sites. The 3C-SiC structure is named according to the repeating sequence of ABC, 4H-SiC is ABCB and 6H-SiC is ABCACB. Figure 2.2 shows primitive cells and basic translation vectors of cubic and hexagonal SiC.

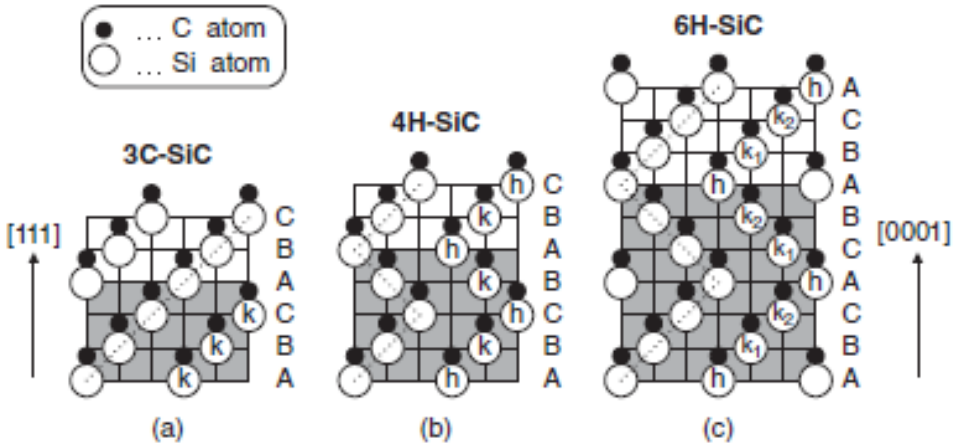
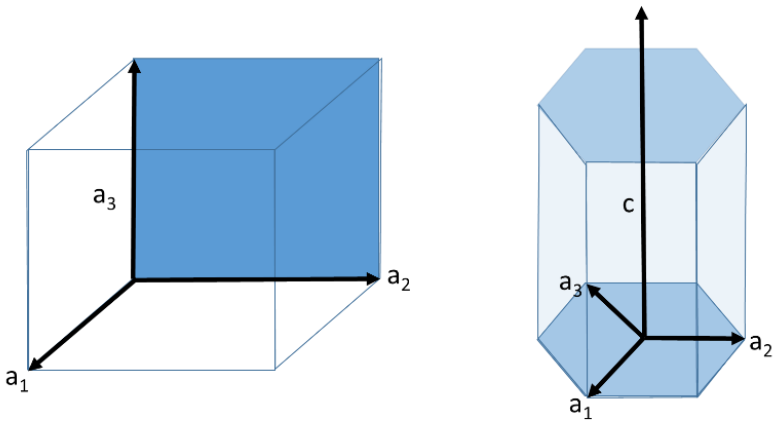


Figure 2.1: Schematic structures of the most common SiC polytypes (a) 3C-SiC, (b) 4H-SiC and (c) 6H-SiC. Open and closed circles represent Si and C atoms respectively [7].



(a) Cubic SiC (b) Hexagonal SiC

Figure 2.2: Primitive cells and basic translation vectors of (a) cubic and (b) hexagonal SiC [7].

The stability and nucleation of SiC polytypes strongly depends on temperature [20]. For instance, the 3C-SiC polytype is not stable and is easily converted to the 6H-SiC polytype at very high temperatures, above 2000 °C [21]. Hence, 4H-SiC and 6H-SiC are popular and preferable polytypes due to their temperature stability. However, 3C-SiC is the only polytype that can be grown on Si substrates [22, 23].

Table 2.1 summarises the physical properties of the major polytypes of 3C-SiC, 4H-SiC and 6H-SiC at room temperature [7]. Among them, 4H-SiC demonstrates the widest bandgap of 3.26 eV followed by 6H-SiC and 3C-SiC at 3.02 and 2.36 eV respectively. Similar to Si, the bandgaps in all of these SiC polytypes decreases with increasing temperature [11]. The electron mobility perpendicular to c-axis of 4H-SiC is more than double compared to that in 6H-SiC. Furthermore, 4H-SiC exhibits an outstanding value of electron mobility along the c-axis of 1200 cm^2/V.s, which is the main reason why 4H-SiC is the most striking polytype. Electron and hole saturated drift velocities for all three polytypes are relatively similar. Even though the critical electrical field along the c-axis of 6H-SiC is higher than that in 4H-SiC, it demonstrates poor electron mobility compared to 4H-SiC. Based on these comparisons, 4H-SiC is the most attractive candidate and suitable for development for power electronic devices.

Properties/Polytype	3C-SiC	4H-SiC	6H-SiC
Bandgap (eV)	2.36	3.26	3.02
Electron mobility perpendicular to c-axis ($cm^2/V.s$)	1000	1020	450
Electron mobility parallel to c-axis ($cm^2/V.s$)	1000	1200	100
Hole mobility ($cm^2/V.s$)	100	120	100
Electron saturated drift velocity (cm/s)	2×10^7	2.2×10^7	1.9×10^7
Hole saturated drift velocity (cm/s)	1.3×10^7	1.3×10^7	1.3×10^7
Critical electric field perpendicular to c-axis (MV/cm)	1.4	2.2	1.7
Critical electric field parallel to c-axis (MV/cm)	1.4	2.8	3.0
Relative dielectric constant ε_s perpendicular to c-axis	9.72	9.66	9.66
Relative dielectric constant ε_s parallel to c-axis	9.72	10.32	10.03

Table 2.1: Physical properties of 3C-SiC, 4H-SiC and 6H-SiC polytypes at room temperature [7].

2.2 SiC MOS Interface Challenges

The success of Si CMOS technology is in no small part due to the fact that a dielectric such as SiO_2 can be easily grown on the Si surface. While SiC can be oxidized to form a SiO_2 dielectric layer, the quality of SiC/SiO_2 interface is poor compared with Si/SiO_2. The deposition of SiO_2 and other dielectrics on either Si or SiC also leads to a poor dielectric interface, containing high levels of charged defects.

Unlike Si thermal oxidation, C is released during SiC thermal oxidation, for example as CO or CO_2 gases as shown in equations 2.1 and 2.2:

$$SiC + {}^{3}/_{2}\, O_2 \rightarrow SiO_2 + CO \quad (2.1)$$

$$SiC + 2O_2 \rightarrow SiO_2 + CO_2 \quad (2.2)$$

However, a small volume of C remains close to the SiO_2/SiC interface according to equation 2.3:

$$SiC + O_2 \rightarrow SiO_2 + C \quad (2.3)$$

This will cause the interface quality to deteriorate and this phenomenon is anticipated to be the source of the high density of interface traps (D_{it}) that minimize the carrier mobility. Possibilities include some combination of the following:

i. C incorporated into the growing SiO_2 layer
ii. C injected into the SiC substrate
iii. C becomes an isolated interstitial
iv. C reacts with excess O
v. C forms complex clusters involving C, O and Si

The mechanism of the chemical reactions is illustrated in Figure 2.3.

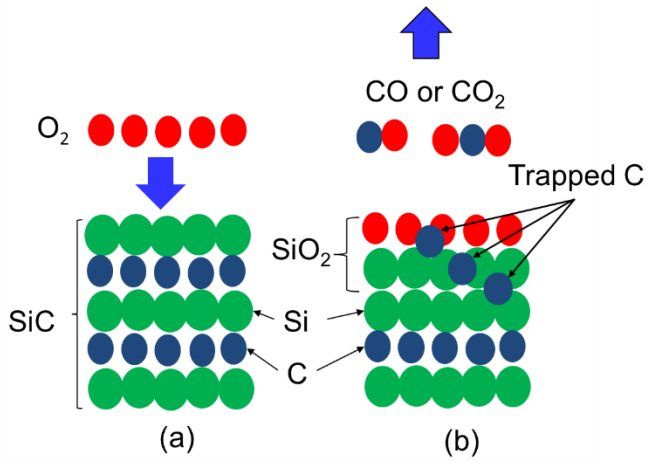


Figure 2.3: Schematic images of C trapping mechanism (a) before and (b) after thermal oxidation where potentially trapped C atoms remain in the SiC.

High resolution transmission electron microscopy (HRTEM) shows the existence of nm-scale transition layers at the 4H-SiC/SiO_2 interface as shown in Figure 2.4(a) [24, 25]. For a 62 nm thermally grown SiO_2 layer, Electron Energy Loss Spectroscopy (EELS) data in Figure 2.4(b) confirms non-stoichiometric behaviour in ratio of C/Si extending 3.3 nm into the 4H-SiC. This can mean that an excess of C or a deficit of Si in the 4H-SiC occurs. Specific defect

identities cannot be assigned from this data, but C interstitials, ternary SiO_xC_y phases and amorphous 4H-SiC are possible explanations. Graphitic features are detected on 4H-SiC surfaces following oxidation and etching using Raman spectroscopy [26], which could correspond with C clusters in 4H-SiC.

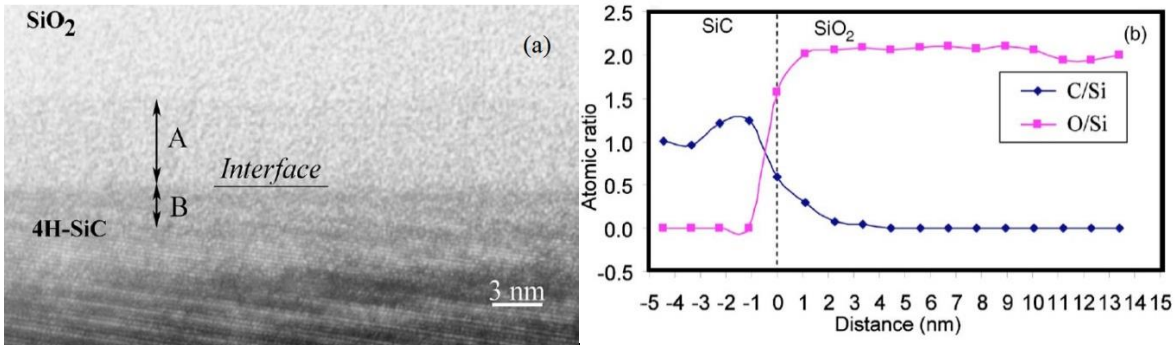


Figure 2.4: (a) A high resolution transmission electron microscope (HRTEM) image showing transition layers appearing on both sides of the 4H-SiC/SiO_2 interface (A extending 4.8 nm into SiO_2 and B 3.3 nm in to 4H-SiC) and (b) C/Si and O/Si ratios profile measured by EELS [25].

2.3 MOS Interface Development

2.3.1 High temperature oxidation

In Si device technology, oxidation is typically performed at a temperature between 800–1100 °C. The thermal oxidation of 4H-SiC initially mimicked Si technology, but with an upper temperature limit of 1200 °C due to the slower rate of oxidation. It was then suggested that oxidation at 1300 °C could offer a decrease in C content, and indeed it was observed that such oxidations led to lower values of D_{it} [27]. The reason suggested was that a higher oxidation rate of C than Si occurred at these elevated temperatures, leading to the rapid removal of C from the interface [28].

There has been evidence to suggest that using even higher temperatures up to 1600 °C may offer additional benefits. A reduction in D_{it} has been observed for MOS capacitor structures thermally oxidised at both 1500 °C and 1600 °C. It has also been highlighted that, as well as a higher temperature being important, so is the ratio of oxygen present in an oxidizing ambient. When incorporated into a lateral MOSFET structure utilizing a p-type epitaxial layer, a 1500 °C anneal managed to yield a channel mobility of 40 cm^2/Vs, demonstrating the potential of this technique [29].

Work on oxidation temperatures ranging from 1200–1700 °C has shown an optimum temperature of 1450 °C for obtaining the lowest D_{it} value in this temperature range [30]. 1700

°C is deemed unreasonable as this is too close to the melting point of silica. Unintentional oxide growth can take place in the cooling period after high temperature thermal oxidation, showing the importance of the gas flow during and also after oxidation. SIMS and XPS have shown that in thermally grown oxides at higher temperature, a thinner transition layer is observed, which is suggested to be the reason for reduced D_{it} under these conditions [31]. Combining high temperature oxidation with a suitable post-oxidation anneal (POA) has shown improvements in D_{it} and mobility values [32].

2.3.2 Low temperature oxidation

Shen and Pantelides [33] proposed the formation of immobile C di-interstitial defects $(C_i)_2$ in 4H-SiC as a result of thermal oxidation. Defects of this kind would go some way to explaining the poor channel mobility observed in many 4H-SiC MOSFETs fabricated with a high thermal budget, even following POA. Low temperature oxidation offers a route to decreased C-related defects by reducing the thickness of the grown SiO_2. This approach requires in addition the deposition of a gate dielectric to avoid gate leakage current.

Hatayama *et al.* [34] reported field effect mobility values as high as 294 $cm^2/V{\cdot}s$ in 4H-SiC MOSFETs utilising a 0.7 nm thick SiO_2 grown at low temperature between the 4H-SiC and a deposited Al_2O_3 dielectric. They concluded that an interfacial oxide layer with a thickness above 2 nm degrades the interface and channel mobility. Figure 2.5 shows the transfer characteristics (I_D-V_{GS}) and corresponding electron mobility of these MOSFETs.

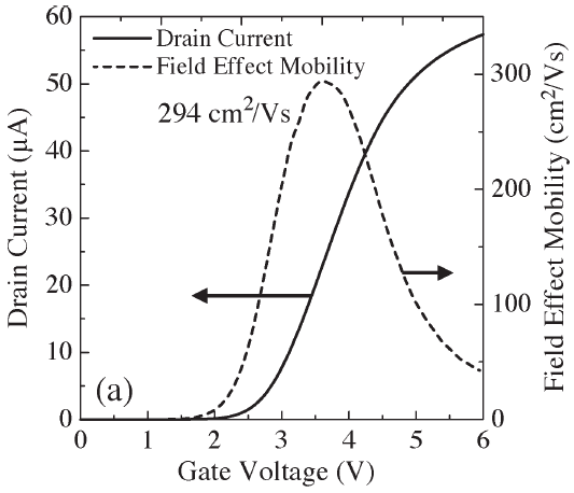


Figure 2.5: I_D-V_{GS} transfer curve and field effect mobility by utilizing a low temperature oxidation technique [34].

In addition, Kim *et al.* [35] have grown SiO_2 layers for MOS capacitors using direct plasma-assisted oxidation at room temperature. They claimed that, because the oxidation reaction mechanisms are different, the concentration of silicon oxycarbides (SiO_xC_y) is substantially reduced compared to thermally grown SiO_2, and that this leads to an improved value of D_{it} ~10^{11} cm^{-2}/eV.

2.3.3 Post oxidation annealing

Performing POA in a particular gas ambient at temperatures of around 900–1400 °C after oxide formation is another method used to enhance oxide/4H-SiC interface quality and thus to improve electron mobility. One of the most promising POA methods is nitridation, which is employed in nitrogen (N)-rich gases such as nitric oxide (NO) [36, 37], nitrous oxide (N_2O) [38, 39] or NH_3 [40, 41]. Chung *et al.* [36] demonstrated an improvement in electron mobility from single digits in as-grown oxide to as high as 37 cm^2/V.s after POA in NO at 1175 °C for 2 hr. During the nitridation process, N effectively passivates interface traps by forming strong bonds with either dangling or strained Si bonds. In addition, the residual clustered C produced during thermal oxidation is also effectively passivated [42, 43]. Yoshioka *et al.* [44] obtained minimum values of interface traps via nitridation in NO at 1250 °C for 70 min, which produced a nitrogen concentration of 3.0 × 10^{14} cm^{-2} as shown in Figure 2.6.

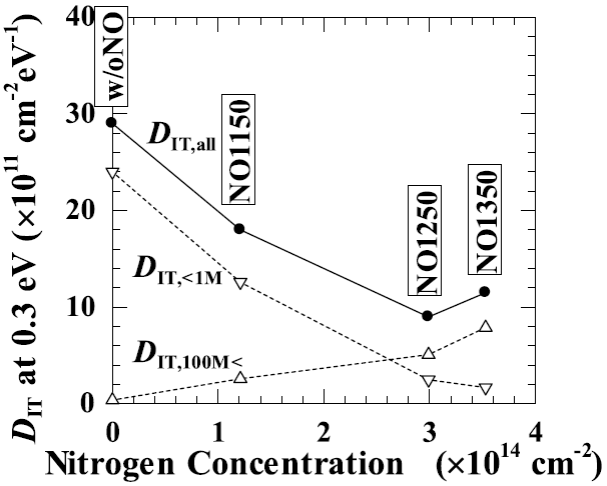
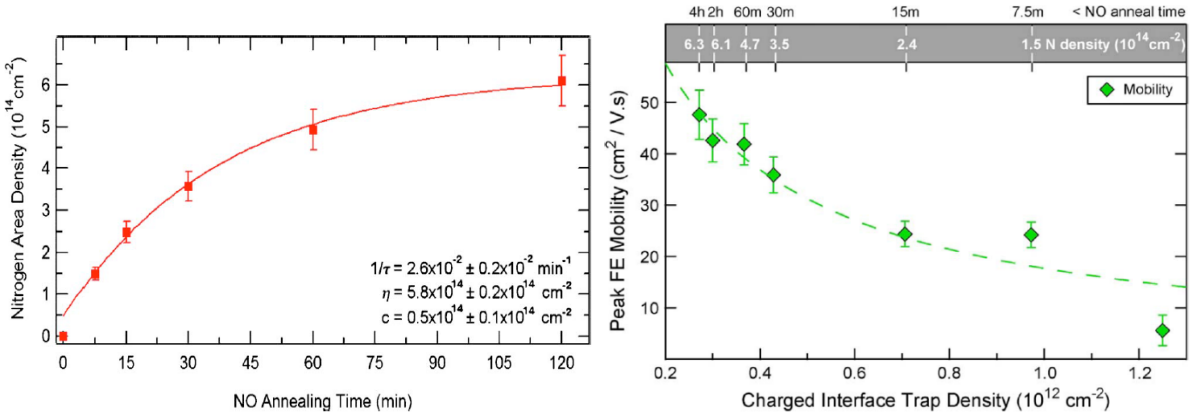


Figure 2.6: Values of D_{it} at Ec = -0.3 eV as a function of nitrogen concentration with different NO annealing times [44].

To further investigate the correlation between N atom concentration and electron mobility, Rozen *et al.* reported that N was saturated at the interface after NO annealing for 2 hr at 1175 °C as shown in Figure 2.7(a). As a result, the peak field effect mobility increases as the D_{it} are

reduced with higher N concentrations as shown in Figure 2.7(b). High densities of N atoms are required to effectively passivate the interface traps and hence increase electron mobility.



(a) (b)

Figure 2.7: (a) Nitrogen concentration by SIMS [45] and (b) peak field effect mobility versus NO annealing time at 1175 °C [46]

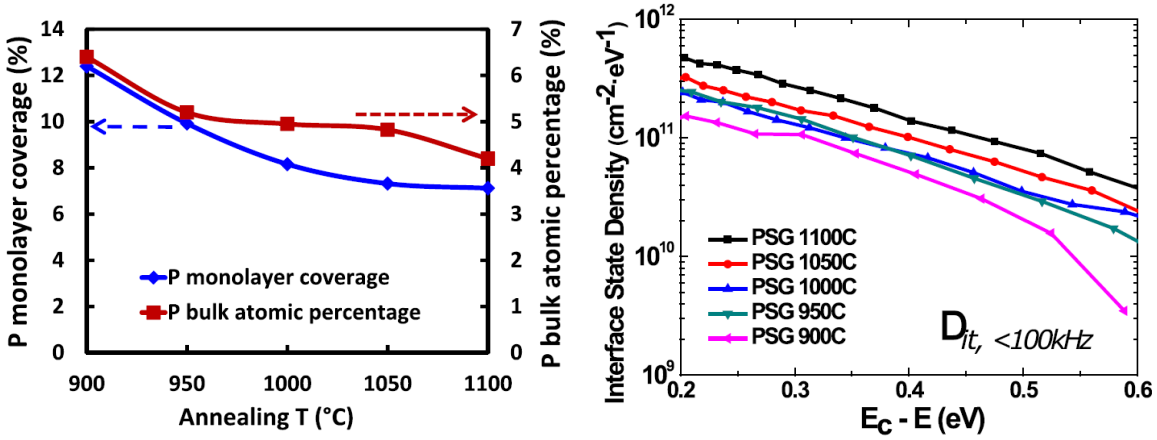
However, NO gas is highly toxic and Lipkin *et al.* [38] proposed POA in N_2O as an alternative solution. Furthermore, Jamet *et al.* [47] revealed that POA either with NO or N_2O produced almost identical effects at the interface due to the fact that N_2O completely decomposes into NO and N_2 gases at a temperature of around 950 °C in the furnace, as shown in the following reactions [7, 48, 49]:

$$N_2O \rightarrow N_2 + O \tag{2.4}$$

$$N_2O + O \rightarrow 2NO \tag{2.5}$$

Another effective technique to reduce interface traps and enhance electron mobility is via POA in phosphoryl chloride ($POCl_3$) [50]. Peak field effect mobility as high as 89 cm^2/V.s was achieved in MOSFETs which underwent $POCl_3$ annealing at 1000 °C, and this level was further improved to 101 cm^2/V.s with multi-step $POCl_3$ annealing [51]. The conversion of thermally grown SiO_2 into phosphosilicate glass (PSG) during $POCl_3$ annealing can be attributed to the suppression of interface traps and an improvement in channel mobility [52]. Jiao *et al.* [53] reported that the percentage of phosphorus (P) distribution in the channel region depends on the $POCl_3$ annealing temperature, as depicted in Figure 2.8(a). The distribution of D_{it} decreases with higher P coverage at the interface and in the PSG bulk. The lowest value of D_{it} was achieved after 900 °C $POCl_3$ annealing as displayed in Figure 2.8(b). However, it is well recognised that PSG gate oxide has a polarization effect and thus a gate instability issue arises with higher P uptake at the interface [53]. One of the main reasons for this is the presence

of oxide traps in the PSG and near the interface traps, which cause trapping and de-trapping effects [54, 55].



(a) (b)

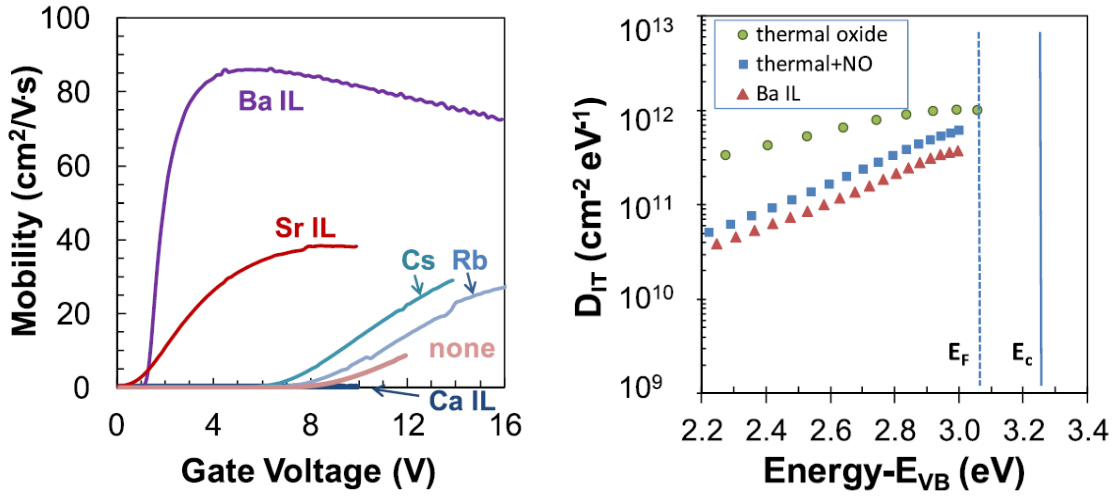
Figure 2.8: (a) Concentration of phosphorus atoms concentration at the interface and in PSG bulk (b) D_{it} distribution of energy levels with different $POCl_3$ annealing temperature [53].

POA in boron (B) gas is another alternative used to passivate interface traps and improve electron mobility in 4H-SiC MOSFETs. By a similar mechanism to that with PSG, thermally grown SiO_2 is converted into borosilicate glass (BSG) by a two-step annealing process. A field effect mobility of 102 $cm^2/V.s$ has been obtained with a low D_{it} value of 9.0×10^{11} cm^{-2}/eV^{-1} [56]. B atoms were uniformly distributed in the oxide and effectively passivated the active interface traps. The improvement in electron mobility has been suggested to be due to stress relaxation in the SiO_2 structure [56]. Recently, Cabello *et al.* [57] reported peak electron mobility as high as 160 $cm^2/V.s$ with a nitrided gate oxide followed by B annealing. Relatively good threshold voltage (V_{th}) control was observed under positive and negative bias stress instability testing at room temperature with boron annealed gate oxide. However, a concern arose concerning the nature of B doped SiO_2, where an electron trapping effect may occur in the oxide bulk [54, 55].

2.3.4 Other methods

The use of "Na-contaminated" gate oxide is another technique that exhibits outstanding electron mobility in 4H-SiC MOSFETs. Initially, field effect mobility up to 170 $cm^2/V.s$ was reported using grown oxide in alumina ambient [58]. But, it was later revealed that the oxidation furnace and grown oxide were contaminated with sodium (Na). This suggests that Na ions increase the oxidation rate and reduce the formation of interface traps [59]. However, these mobile Na ions are undesirable as they can diffuse into the gate oxide and cause instability in threshold voltage,

and this behaviour has been well recognised in Si technology [12]. Lichtenwalner *et al.* [60] reported the insertion of the group I alkali elements Rb and Cs and group II alkaline earth elements Ca, Sr and Ba into the channel region of 4H-SiC MOSFETs. A gate stack consisting of an ultrathin layer of Ba (~ 0.6 - 0.8 nm) and 30 nm of deposited SiO_2 produced field effect mobility as high as 85 $cm^2/V.s$ as shown in Figure 2.9(a). The D_{it} distribution also showed a significant reduction compared to that of thermally grown gate oxide as well as NO treated gate oxide. Unlike Na-contaminated gate oxides which contain a large number of mobile ions, the Ba interlayer gate stack demonstrated a consistent V_{th} with a slight hysteresis of 0.8 V during positive bias temperature stress (BTS) measurements. This suggests that the Ba atoms are less mobile and hence become strongly bonded and effectively passivate the interface traps.



(a) (b)

Figure 2.9: (a) Field effect mobility of fabricated 4H-SiC MOSFET and (b) D_{it} distribution from NMOS using Rb, Cs, Ca, Sr and Ba interlayers compared with as grown gate oxide [60].

A counter doped gate oxide is formed by implanting group-VII elements into the channel region of n-channel MOSFETs. This technique was first introduced by Ueno *et al.* [61], where N ions were implanted at the channel region. Channel mobility increased and the V_{th} decreased with increasing N dosage [61]. Instead of direct implantation, this region can also be formed by POA. Fiorenza *et al.* [62] observed heavily doped N and P atoms in the channel region after POA in N_2O and $POCl_3$ using a scanning capacitance microscopy (SCM) probe [62]. The SCM probe also detected an electrically active region underneath the deposited SiO_2 as illustrated in Figure 2.10. Channel mobility as high as 110 $cm^2/V.s$ was obtained using a gate oxide with NO annealing on antimony (Sb) doped at the gate oxide [63].

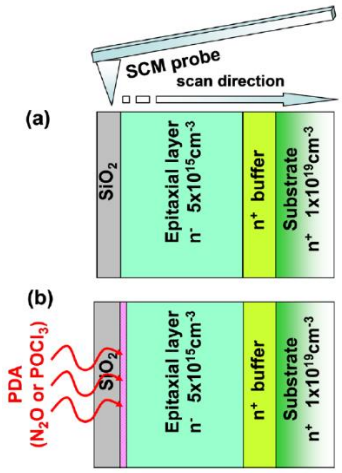


Figure 2.10: Schematic of a cross-section of 4H-SiC MOS capacitor (a) before and (b) after POA in N_2O and $POCl_3$ [62].

The combination of an Sb-rich channel which provides extra electron density and NO annealing passivates the interface traps and enhances electron mobility at the channel. Recently, Yang *et al.* [64] reported that replacing the NO anneal with a boron anneal at 950 °C for 30 min significantly improved field effect mobility to a value of 180 $cm^2/V.s$. However, the high peak channel mobility drops rapidly with increasing gate voltage. Furthermore, BSG gate oxide exhibits relatively high V_{th} hysteresis up to 8 V at 1.5 MV/cm stress at 150 °C during the BTS measurements. The poor BTS performance is suggested to be due to the large concentration of oxide traps, which is a characteristic of BSG gate oxide [54].

Different distributions of interface traps have been observed when different crystal faces of off-axis 4H-SiC are employed. The most commonly reported crystal faces other than the typical "Si face" (0001) crystal faces are the off-axis 4H-SiC $(000\bar{1})$ "C face", the on-axis 4H-SiC $(11\bar{2}0)$ "A face" and the $(1\bar{1}00)$ "M face". Figure 2.11 shows the major crystal faces of 4H-SiC.

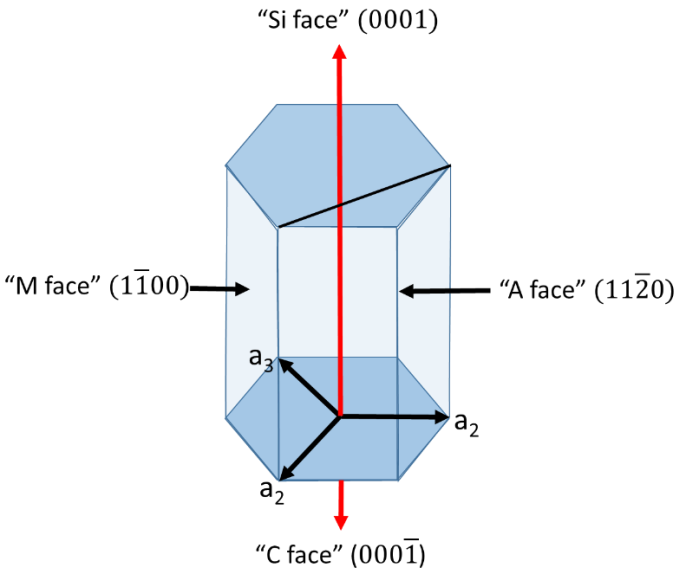
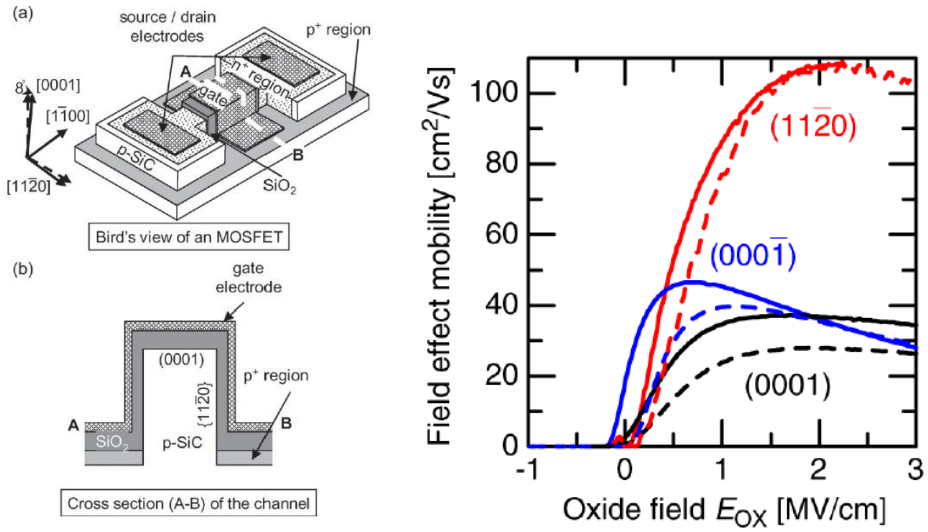


Figure 2.11: Crystal faces of 4H-SiC

Various crystal faces exhibit different behaviour due to the different polar structures from face to face. Side-wall channels on the "A face" exhibit a field effect mobility of 42 $cm^2/V.s$, which is 2× and 3× higher compared to the "M face" and "Si face" respectively with deposited SiO_2 followed by NO annealed gate oxide [65]. The combination of these crystal faces produces 16× higher current carrying capability compared to the conventional planar MOSFET with a similar oxidation process due to the higher channel mobility on the "A face" and "M face". A schematic illustration of fabricated 3D gate oxide is shown in Figure 2.12(a-b). Peak channel mobility up to 108, 37 and 46 $cm^2/V.s$ for the "A face", "M face" and "Si face" respectively using thermally grown SiO_2 with subsequent NO annealing at 1300 °C for 80 min has been demonstrated as shown in Figure 2.12(c) [66]. The channel mobility values of the devices with the NO annealed gate oxide are higher than those with N_2O annealed gate oxide for the "Si face" and "C face". But similar high channel mobility was observed for the "A face" regardless of nitridation conditions. However, the grown oxide thickness is not uniform on each of the crystal faces due to different growth rates, and hence it is difficult to control the V_{th} value, one of the solutions to obtain a uniform oxide thickness is to deposit the oxide via ALD. However, high leakage current and interface quality are still major problems which need to be resolved with this system.



(c)

Figure 2.12: (a-b) 3D gate structure MOSFETs [65] and (c) Field-effect mobility as a function of oxide field for 4H-SiC MOSFETs with different crystal orientation anneal in NO (solid line) and N_2O (broken line) [66]

Lichtenwalner *et al*. [67] reported electron mobility as high as 106 $cm^2/V.s$ with a gate stack consisting of an ultrathin layer of SiO_2 (~ 1.8 nm) and 25 nm of deposited Al_2O_3 using ALD. Prior to Al_2O_3 deposition, a thin SiO_2 layer was grown by NO annealing at 1175 °C for 20 min to control the formation of interface traps. A slight V_{th} shift of 0.7 V was observed after the second I_D - V_{GS} sweep due to electron trapping in the gate oxide as shown in Figure 2.13. In addition, Yang *et al.* [68] proposed the insertion of an ultrathin layer (~ 1 nm) of La_2O_3 between the ALD deposited SiO_2 with 4H-SiC. A high channel mobility of 133 $cm^2/V.s$ was obtained with 3× larger current carrying capability compared to the gate oxide without La_2O_3 as shown in Figure 2.14. In both cases [67, 68] in which an ultrathin layer was inserted between the oxide deposited by ALD and 4H-SiC relatively high peak electron mobility (>100 $cm^2/V.s$) were found, but these dropped rapidly with increasing electric field. However, since ALD provides uniform oxide thickness, these techniques may be suitable for 3D MOSFET implementation.

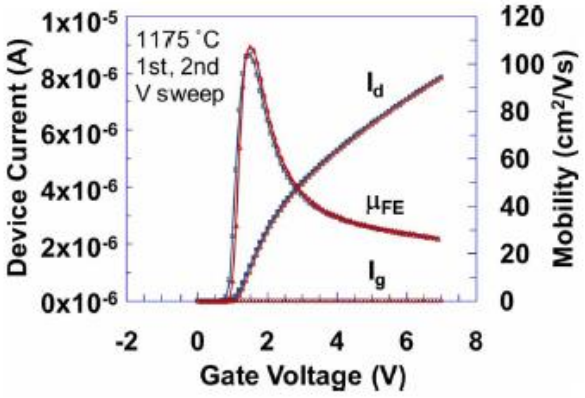


Figure 2.13: First and second sweeps of I_D - V_{GS} characteristics for MOSFETs with gate oxide growth at 1175 °C in NO and followed by Al_2O_3 ALD deposition [60].

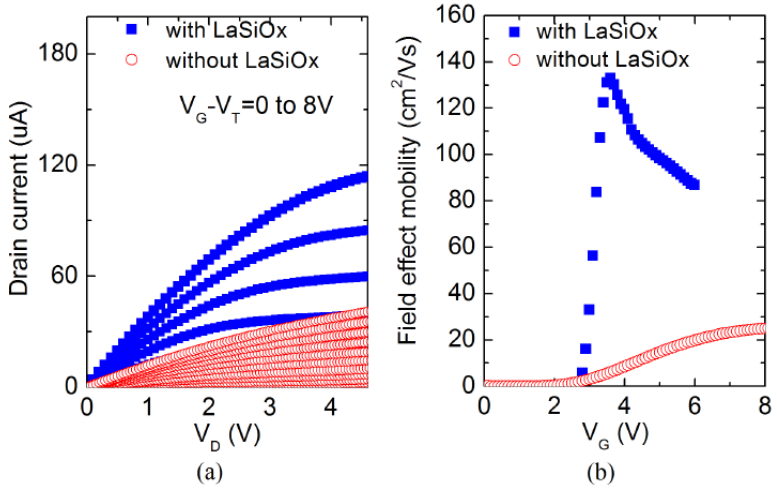


Figure 2.14: MOSFET fabricated with and without the insertion of $LaSiO_x$ between deposited SiO_2 and 4H-SiC (a) I_D - V_{DS} curve and (b) field effect mobility versus gate voltage [68].

To date, encouraging improvements have been achieved in increasing channel mobility in 4H-SiC MOSFETs. Table 2.2 and Figure 2.15 show reports of the current status of field effect mobility as a function of D_{it} at 0.2 eV below the conduction band edge. However, the values of peak channel mobility of 4H-SiC MOSFET still lag far behind those achieved by Si MOSFETs.

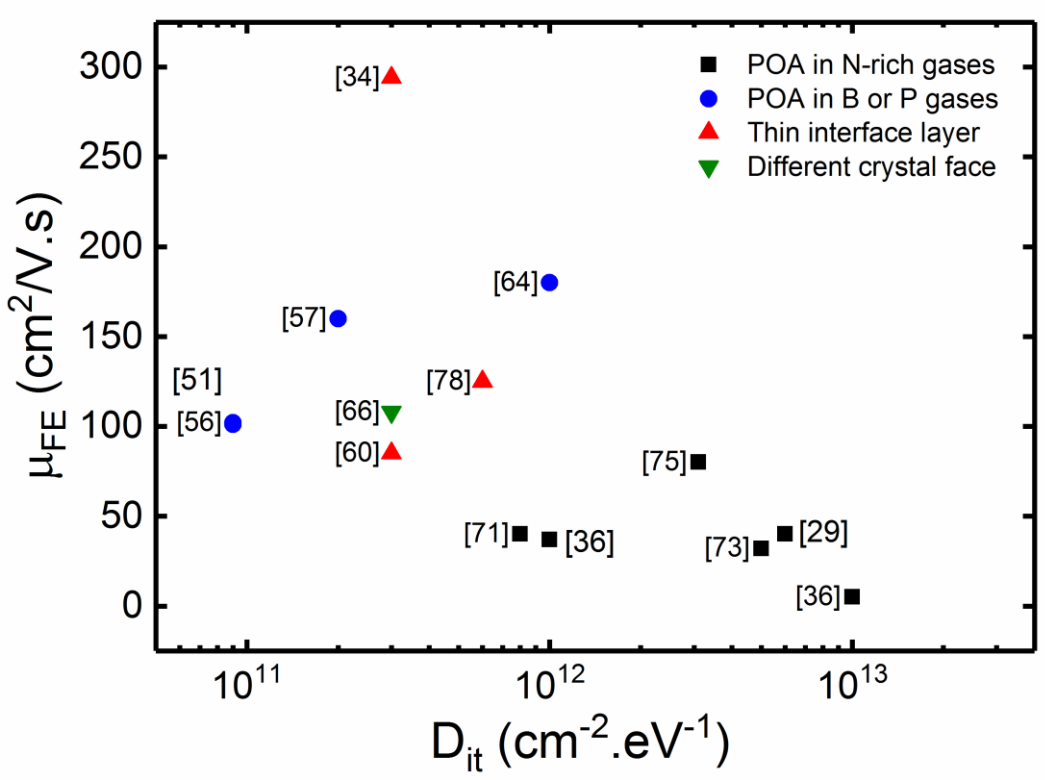


Figure 2.15: Current status of field effect mobility as a function of D_{it} at 0.2 eV near to the conduction band edge with different gate oxide formation methods.

Year	Oxidation	Annealing/doped at channel	Doping concentration (cm^{-3})	D_{it} ($cm^{-2}eV^{-1}$) at Ec-E=0.2 eV	μ_{FE} (cm^2/Vs)	Reference
1994	(Si) Dry O_2 at 900 °C	H_2 anneal at 450 °C	3.9×10^{15}	~ 10^9	805	[12, 69]
1998	Dry O_2 at 1050 °C for 5 min + wet O_2 at 1050 °C for 265 min + dry O_2 at 1050 °C for 5 min	N_2 anneal at 1100 °C for 400 min + Ar anneal at 1100 °C for 60 min + N_2 anneal at 950 °C for 60 min	2.5×10^{15}	-	165	[70]
2001	Dry O_2 at 1200 °C for 2.5 hr + Ar at 1200 °C for 1 h + wet O_2 at 950 °C for 3 h	N/A	1×10^{16}	1.0×10^{13}	5	[36, 37]
2001	Dry O_2 at 1200 °C for 2.5 hr + Ar at 1200 °C for 1 h + wet O_2 at 950 °C for 3 h	NO anneal at 1175 °C for 2 hr	1×10^{16}	1.0×10^{12}	37	[36, 37]
2005	Dry O_2 at 1200 °C for 2 hr and 1000 °C for 6 hr	Al doped at channel + N_2 anneal at 1000 °C "Sodium contamination"	5×10^{15}	-	170	[58]
2006	Dry O_2 at 1050 °C for hr	SiO_2-TEOS deposited + Ar anneal for 1 hr	5×10^{16}	8.0×10^{11}	40	[71]
2007	Dry O_2 at 1150 °C for 4 hr	H_2 at 500 °C for 1 h	~ 10^{16}	1.0×10^{12}	-	[72]
2008	Deposited SiN_x at 400 °C	N_2O anneal at 1300 °C for 5 min	8×10^{15}	5.0×10^{12}	32	[73]
2008	Deposited Al_2O_3 at 190 °C	No	7.6×10^{15}	-	64	[74]
2008	Dry O_2 at 600 °C for 3 min + deposited Al_2O_3	No	7.6×10^{15}	$3\text{-}5 \times 10^{11}$	294	[34]

2009	Deposited SiO_2	N_2O anneal at 1300 °C for 30 min	7.8×10^{15}	-	42 $(11\bar{2}0)$ 21 $(1\bar{1}00)$	[65]
2009	Deposited Al_2O_3	NO anneal in at 1175 °C for 20 min + Deposited Al_2O_3 + N_2 anneal at 300 °C for 60 s	-	-	106	[67]
2010	Deposited SiO_2 + 1175 °C for 3.5 h	Nitrogen doped at channel before oxidation	5×10^{15}	3.1×10^{12}	80	[75]
2010	Dry O_2 at 1200 °C for 160 min	$POCl_3$ anneal at 1000 °C for 10 min	7×10^{15}	9.0×10^{10}	101	[50, 51]
2011	Dry O_2 at 1150 °C for 3 hr	N_2O anneal at 1300 °C for 2 hr + Ar anneal at 1300 °C for 30 min	6×10^{15}	-	33	[76]
2013	Dry O_2 at 1150 °C	NO anneal at 1300 °C for 80 min	4-6 $\times 10^{15}$	3.0×10^{11} $(11\bar{2}0)$	46 $(000\bar{1})$ 108 $(11\bar{2}0)$	[66, 77]
2014	Dry O_2 at 1200 °C for 170 min	Boron anneal at 950 °C for 10 min + Ar anneal at 950 °C for 120 min	1×10^{16}	9.0×10^{10}	102	[56]
2014	Dry O_2 at 1150 °C for 11 hr	Sb doped at channel (6×10^{12} cm^{-2}) + N_2O anneal at 1175 °C for 30 min	6×10^{15}	-	110	[63]
2014	Dry O_2 at 1500 °C	No	1×10^{17}	6.0×10^{12}	40	[29]
2014	Deposited SiO_2	Deposited ultrathin Barium + O_2 anneal at 900 °C for 1 h + Deposited SiO_2 + N_2	5×10^{15}	3.0×10^{11}	85	[60]

		anneal at 900 to 950 °C for 1–10 h				
2015	Deposited SiO_2	Deposited 1 nm of La_2O_3 + Deposited SiO_2 + N_2O anneal at 900 °C	5×10^{15}	-	133	[68]
2017	Deposited TEOS after surface treatment	N_2O anneal + Boron anneal at 950 °C and 1150 °C for 30 min	7×10^{15}	2.0×10^{11}	160	[57]
2017	Dry O_2 at 1150 °C	Sb doped at channel + Boron anneal at 950 °C for 30 min	1×10^{16}	1.0×10^{12}	180	[64]
2018	Dry O_2 at 600 °C for 3 min + deposited Al_2O_3	N_2 anneal at 300 °C for 60 min	5.3×10^{15}	6×10^{11}	125	[78]

Table 2.2: Summary of oxidation process with extracted D_{it} and field effect mobility of 4H-SiC MOSFET

2.4 Summary and Conclusion

The early evolution of SiC and its development in the semiconductor industry has been discussed. An exceptional polytypism phenomenon is found with SiC structures, and these offer outstanding and unique electrical and physical properties. As Si-based power device technology is relatively mature and it is difficult to achieve any further breakthroughs, SiC is seen as an attractive alternative. It is wide bandgap and the ability to grow SiO_2 layers from its bulk are the main reasons why SiC, particularly 4H-SiC, is chosen and has attracted the attention of many researchers. However, SiO_2/4H-SiC interface quality is still poor and needs to be addressed. Unlike with Si, the thermal oxidation of 4H-SiC generates a number of C atoms trapped at the interface and/or inside the 4H-SiC and SiO_2. These trapped C atoms are immobile and tend to combine with each other to form a large concentration of C clusters such as $(C_i)_2$ and thus the interface quality deteriorates. These undesired C defects compromise electron movement at the SiO_2/4H-SiC interface of MOSFETs, which leads to low channel mobility.

A lot of effort has been put into solving this problem, for example by oxidation at extremely high temperatures to get rid of the C defects, but the resulting electron mobility is still disappointing. POA in a nitridation atmosphere is a commonly used technique but could only produce channel mobility in the range of 30-40 cm^2/Vs. Other POA techniques such as using B and P gases have exhibited channel mobility above 100 cm^2/V.s, but then a problem related V_{th} instability has arisen. Similar problems also happen with Na-contaminated MOSFETs where the mobile Na ions diffuse into the gate oxide leading to device instability. Recently, a counter-doped channel has been proposed to increase the density of carrier concentration and thus increase electron mobility, but BTS testing showed that the gate oxide consists of high concentrations of oxide traps which lead to a large hysteresis between the forward and reverse bias sweeps at high temperature. Instead of the commonly used Si face, other faces have also been investigated and used to form the gate channel, but increased surface roughness due to the etching process to reach the other faces has caused degradation.

But the insertion of a thin SiO_2 layer grown between the deposited oxide and 4H-SiC has produced high electron mobility values and seems promising. This approach is investigated in this thesis [78]. Rather than trying to mitigate the effect of the excess C resulting from thermal oxidation of 4H-SiC to form a MOSFET gate stack, minimising the formation of excess

C by minimising the thermal oxidation of 4H-SiC is an effective method. Peak electron mobility as high as 300 $cm^2/V.s$ has been reported utilising a grown thin SiO_2 with subsequent Al_2O_3 deposition as a gate stack.

In conclusion, in order to produce high channel mobility in MOSFETs, the oxidation must be sufficient to grow ultrathin SiO_2 with relatively solid Si-O bonds. Muller *et al.* [79] have set an absolute minimum thickness for an ideal SiO_2 gate dielectric which is four Si atoms across or 0.7 nm in terms of physical thickness. Then, by depositing a thicker dielectric using Al_2O_3 on top of the ultrathin layer of SiO_2, any ensuing gate leakage can be mitigated without an appreciable decrease in capacitance owing to the high dielectric constant of Al_2O_3. In this way, the dielectric reliability originating from tunnelling mechanisms is avoided, thus prolonging device lifetime.

Chapter 3

Device Fundamentals, Fabrication and Characterisation

3.1 Introduction

The success of semiconductor electronic devices in Silicon (Si) CMOS technology is mainly due to the understanding of the physics in Metal Oxide Semiconductor (MOS) devices. The fabrication process of MOS devices is critical in determining their performance. A number of methods can be applied to fabricate MOS devices, although defects and traps which may occur at the oxide-semiconductor interface greatly influence the performance. In Si MOS devices, techniques to mitigate such traps have been developed after extensive efforts. However in SiC, the problem of traps, particularly at the interface, has still not been resolved. A suitable fabrication technique has yet to be developed to solve this problem as has been achieved with Si. The key objective of this thesis is to produce high performance MOS devices in term of low concentrations of interface traps and high electron mobility, as well as high reliability and stability. In this chapter, the fundamentals, characterisation and fabrication techniques for 4H-SiC MOS devices are discussed. The methods used for electrical and physical characterisation are also explained in detail.

3.2 MOS Device Fundamentals

Since the most important part of the structure of a MOSFET is the gate-channel-substrate area, extensive studies have been carried out on the basic two-terminal MOS in order to understand the semiconductor interface physics [80]. Typically, stability and reliability issues in MOS devices are related to the surface quality of the semiconductor. In order to produce high performance in MOSFETs, it is important to understand the physics of the semiconductor

surface [12]. Most research has focussed on the fabrication of n-channel MOSFETs (p-substrate) due to their higher electron mobility compared to hole mobility [81].

3.2.1 Ideal p-type MOS capacitors

The p-type MOS capacitor consists of a layer of insulator between the semiconductor and the metal contact as shown in Figure 3.1(a). The contact is either a metal plate or a heavily doped polysilicon layer which acts as a metal for the gate contact. The insulator is an important feature in the device, and it can be formed by deposition or growth. Either silicon dioxide (SiO_2) or a high-k material can be used as the insulator in Si or silicon carbide (SiC) MOS structures. In this explanation, SiO_2 is used as the insulator. The bulk of the device is constantly grounded.

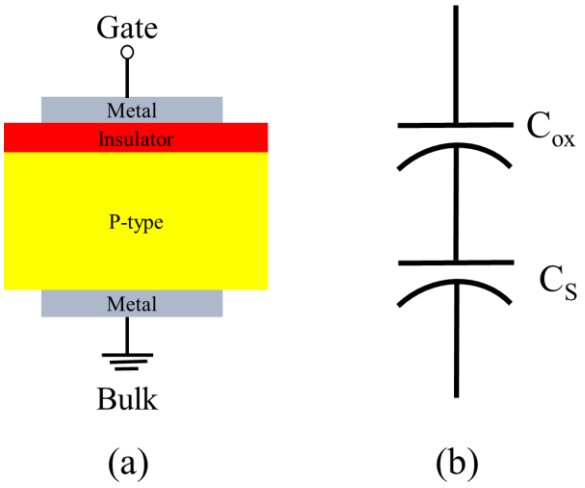


Figure 3.1: MOS capacitor; (a) schematic cross-sectional view and (b) equivalent circuit of total capacitance

The total capacitance of the MOS system is the sum of series capacitance of the oxide capacitance (C_{ox}) and the semiconductor capacitance (C_s) as shown in equation 3.1.

$$\frac{1}{C_{total}} = \frac{1}{C_{ox}} + \frac{1}{C_S} \tag{3.1}$$

To operate the MOS capacitor, a bias voltage (V_G) is applied to the gate contact and thus the charge distribution (Q_s) and surface potential (ψ_s) in the semiconductor can be controlled. Ideally, there is zero current conduction in the oxide as well as no oxide charges present through the oxide or at the oxide-semiconductor interface.

Figure 3.2(a) shows an energy band diagram for a metal, oxide and semiconductor. The energy difference between the Fermi level (E_F) and vacuum level is called the work function (ϕ), where

ϕ_s is for the semiconductor and ϕ_m for metal. The electron affinity (χ) is the difference between the conduction band edge (E_C) and the vacuum level in a semiconductor.

Figure 3.2(b) shows how the energy bands align when the MOS structure is formed. At thermal equilibrium, E_F is constant and the vacuum level is continuous throughout the system. As the work function of both metal and semiconductor are different, the bands are bent downward, assuming $q\phi_m$ is less than $q\phi_s$ and thus $q\psi_s$ is positive. The $q\psi_s$ can be expressed as:

$$q\psi_s = E_{i(bulk)} - E_{i(surface)} \tag{3.2}$$

where $E_{i(bulk)}$ and $E_{i(surface)}$ are the intrinsic Fermi level in the bulk and at the surface of the semiconductor. In this condition, the semiconductor surface is negatively charged since the electron concentration (n_p) increases while the hole concentration (p_p) decreases with decreasing energy difference (E_i-E_F) as expressed in equations 3.3 and 3.4 [12]

$$n_p = n_i \exp\left[-\frac{(E_i - E_F)}{kT}\right] \tag{3.3}$$

$$p_p = n_i \exp\left[\frac{(E_i - E_F)}{kT}\right] \tag{3.4}$$

where n_i is the intrinsic carrier concentration of the semiconductor, k is the Boltzmann constant, T is temperature. In order to achieve the flatband condition, a negative voltage which is equal to the work function difference ($q\phi_{ms}$) is applied to the metal.

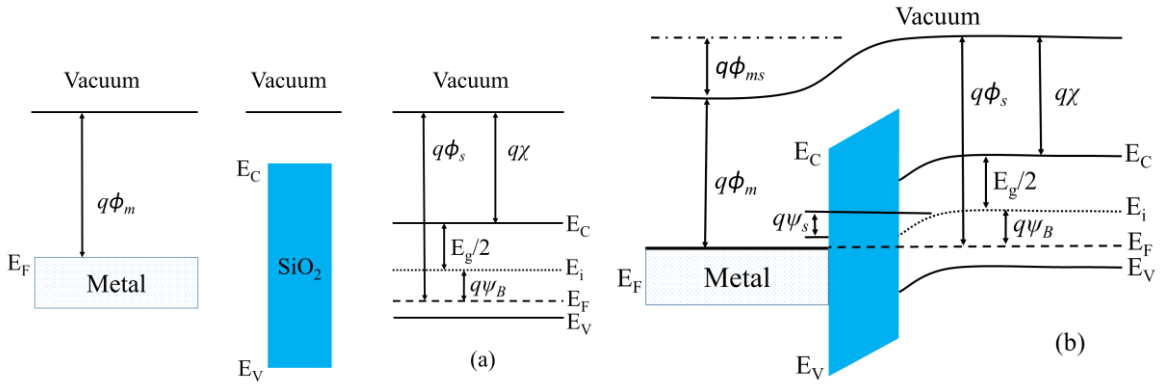


Figure 3.2: (a) Each energy band diagram of the metal, oxide and semiconductor and (b) Energy band diagram of an MOS capacitor at thermal equilibrium.

In this condition, the flatband voltage (V_{fb}) is given by equation 3.5 [12]:

$$V_{fb} = q\phi_{ms} \tag{3.5}$$

where $q\phi_{ms}$ can be expressed by equation 3.6:

$$q\phi_{ms} = q\phi_m - q\phi_s \tag{3.6}$$

$$q\phi_{ms} = q\phi_m - \left(q\chi + \frac{E_g}{2} + q\psi_B\right) \tag{3.7}$$

where

$$\psi_B = \frac{kT}{q}\left(\ln\frac{N_A}{n_i}\right) \qquad \text{for p-type} \tag{3.8}$$

$$\psi_B = -\frac{kT}{q}\left(\ln\frac{N_D}{n_i}\right) \qquad \text{for n-type} \tag{3.9}$$

where q is elementary charge, and N_A and N_D are the electrically active doping concentrations for p-type and n-type semiconductor respectively. The intrinsic carrier concentration (n_i) can be determined as [12]:

$$n_i^2 = N_C N_V \exp\left(-\frac{E_g}{kT}\right) \tag{3.10}$$

where N_C and N_V are the effective densities of states in the conduction and valence bands respectively [12]. The bandgap is temperature dependent and can be semi-empirically expressed as follows [11]:

$$E_g(T) = E_g(0) - \frac{\alpha T^2}{T+\beta} \tag{3.11}$$

where $E_g(0)$ is the bandgap at 0 K, and α and β are fitting parameters ($\alpha = 8.2 \times 10^{-4}$ eV/K, $\beta = 1.8 \times 10^3$ K) [7]. For SiC, the bandgap decreases with temperature as depicted in Figure 3.3.

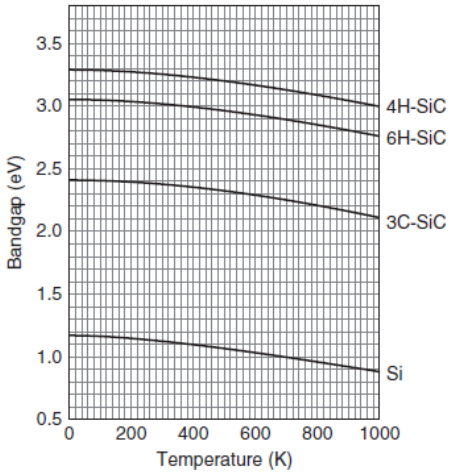


Figure 3.3: Temperature dependence of bandgap for several SiC polytypes [7]

Accumulation

When the applied voltage on the gate is more negative than flatband voltage ($V_G < V_{fb}$), putting negative charges (Q_m) on the gate, the bands near the semiconductor surface are bent upward. The energy band diagram can be illustrated as shown in Figure 3.4. This situation is referred to as the accumulation state, because charge accumulates at the surface such that $p_p > N_A$.

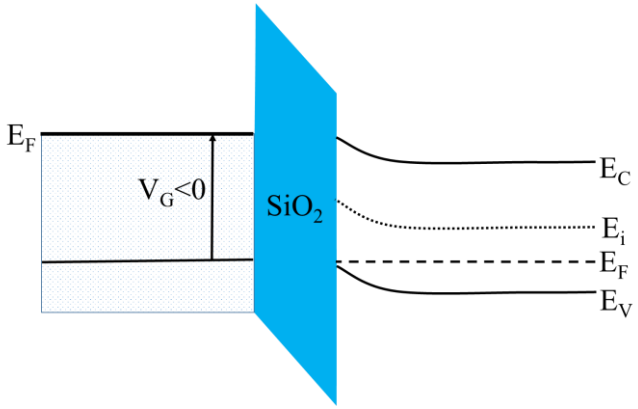


Figure 3.4: Energy band diagram during accumulation state

In this condition, based on equation 3.4, as E_i-E_F increases, the hole concentration is increased at the semiconductor surface and thus positively charged (Q_{acc}). The induced Q_{acc} is equal to Q_m to maintain a balance of the charges as illustrated in Figure 3.5(a). The charges at the semiconductor surface in the accumulation layer can be expressed as equation 3.12 and the charge relationship with applied V_G is shown in Figure 3.5(b).

$$Q_{acc} = -C_{ox}(V_G - V_{fb}) \tag{3.12}$$

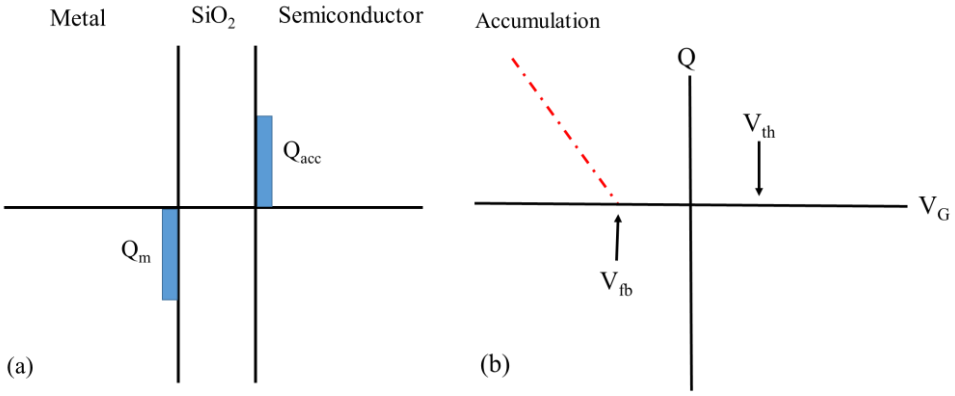


Figure 3.5: (a) Charge distribution and (b) charge versus V_G of p-type MOS capacitor during accumulation state

In the accumulation condition:

$$V_G < V_{fb} \tag{3.13}$$

$$Q_{acc} > 0 \tag{3.14}$$

$$\psi_s < 0 \tag{3.15}$$

Depletion

Next, when a small voltage more positive than flatband voltage ($V_G > V_{fb}$) is applied to the gate, the bands near the semiconductor are bent downward and thus the energy difference (E_i-E_F) decreases. The energy band diagram can be illustrated as shown in Figure 3.6. This situation is referred to as the depletion state, because majority carriers (holes) are depleted from the surface.

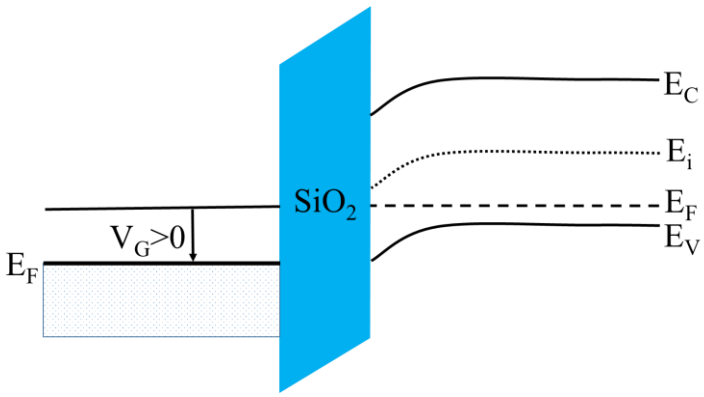


Figure 3.6: Energy band diagram during depletion state

In this condition, based on equation 3.4, as the E_i-E_F decreases, the positive charges (hole) decrease at the semiconductor surface leaving ionized acceptors (negatively charged) as shown in Figure 3.7(a). This space charge (Q_{dep}) in the depletion region can be expressed as:

$$Q_{dep} = -qN_AW \tag{3.16}$$

where N_A is the substrate doping concentration and W is the width of the surface depletion region. The charge relationship with applied V_G is shown in Figure 3.7(b).

In the depletion condition:

$$V_G > V_{fb} \tag{3.17}$$

$$Q_{dep} < 0 \tag{3.18}$$

$$\psi_B > \psi_s > 0 \tag{3.19}$$

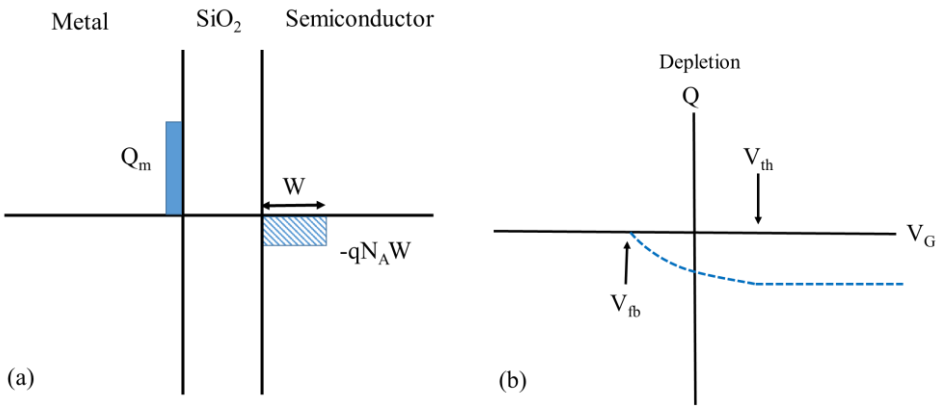


Figure 3.7: (a) Charge distribution and (b) charge versus V_G of p-type MOS capacitor during depletion state

Inversion

Lastly, when a greater positive bias is applied to the gate, the bands at the semiconductor surface are bent downwards more than in the depletion state. The energy band diagram can be illustrated as shown in Figure 3.8.

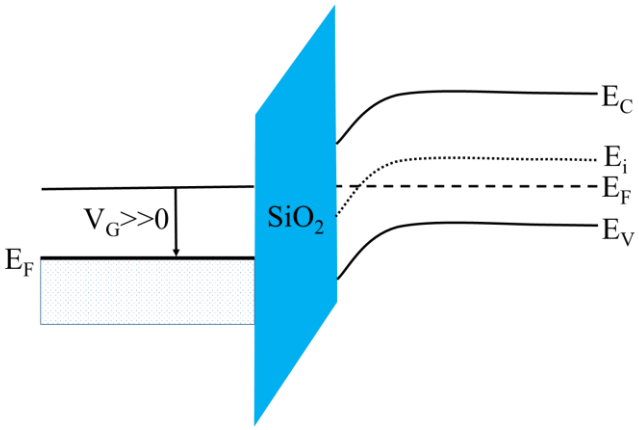


Figure 3.8: Energy band diagram during inversion state

When the applied voltage is high enough so that the E_i at the surface crosses over E_F, the depletion region stops growing and any further increase of voltage will start to induce excess negatively charge (electrons) at the semiconductor surface. In this situation, the bulk "majority" carrier concentration (hole) at the surface is less than the "minority" carrier concentration (electron). Initially, the surface is in weak inversion because the electron concentration is small. Further applied V_G will even bend the bands near the semiconductor surface. The onset of strong inversion occurs when the electron concentration near to the semiconductor surface is equal to the N_A and the ψ_s is defined as:

$$\psi_s = 2\psi_B \tag{3.20}$$

The onset of strong inversion is referred to as threshold voltage (V_{th}). When $n_p > N_A$, the surface is thus inverted and this situation is referred to as inversion condition. The charges can be expressed as equation 3.21 and illustrated as in Figure 3.9(a). The charge relationship with applied V_G is shown in Figure 3.9(b).

$$Q_{inv} = -C_{ox}(V_G - V_{th}) \tag{3.21}$$

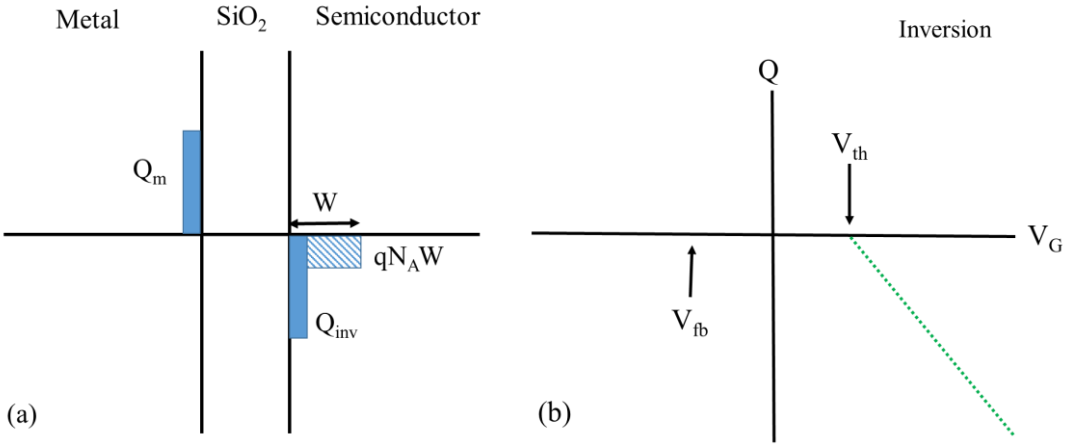


Figure 3.9: (a) Charge distribution and (b) charge versus V_G of p-type MOS capacitor during depletion state

In this inversion condition:

$$V_G > V_{th} \tag{3.22}$$

$$Q_{inv} < 0 \tag{3.23}$$

$$2\psi_B > \psi_s > \psi_B \quad \text{Weak inversion} \tag{3.24}$$

$$\psi_s > 2\psi_B \quad \text{Strong inversion} \tag{3.25}$$

The V_{th} is determined at the onset of strong inversion and can be expressed as in equation 3.26 [12]:

$$V_{th} = V_{fb} + \frac{\sqrt{2\varepsilon_s\varepsilon_o qN_A(2\psi_B)}}{C_{ox}} + 2\psi_B \tag{3.26}$$

where ε_s is the relative permittivity of the semiconductor.

In conclusion, MOS devices can be distinguished by different physical biasing states, including accumulation, depletion and inversion. For an ideal p-type device, accumulation occurs when $V_{GS} < V_{fb}$, depletion when $V_{th} > V_{GS} > V_{fb}$ and inversion when $V_{GS} > V_{th}$. During these conditions, the charge distribution and the corresponding equivalent capacitance-voltage

(C-V) characteristics can be shown as in Figure 3.10. From these three conditions, C-V measurements of the MOS device can be performed for device characterisation as outline in section 3.3.3 [82]. Table 3.1 shows the surface potential characteristics during different conditions.

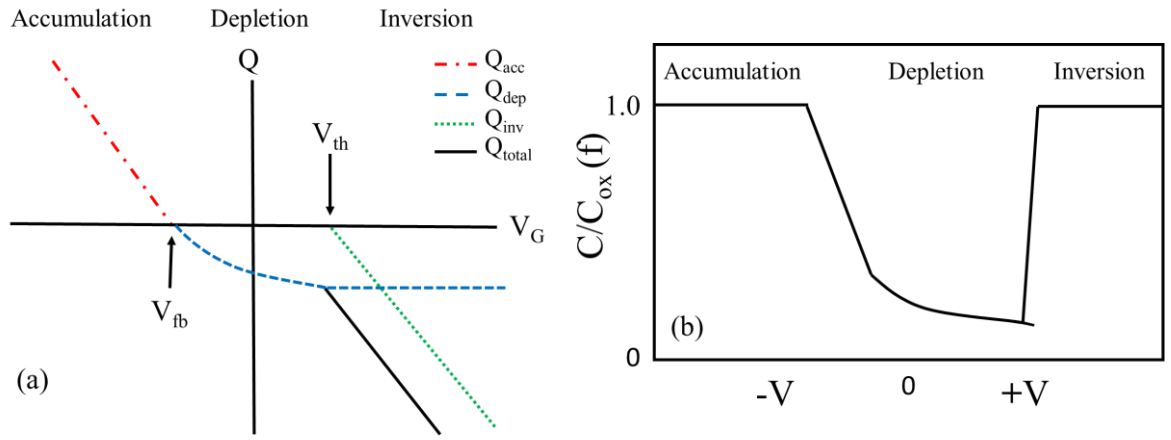


Figure 3.10: (a) Total charges distribution and (b) corresponding C-V characteristics curve during accumulation, depletion and inversion states

Surface potential (ψ_s)	State
$\psi_s < 0$	Accumulation
$\psi_s = 0$	Flatband
$\psi_B > \psi_s > 0$	Depletion
$\psi_s = \psi_B$	Midgap ($n_p=n_i$)
$2\psi_B > \psi_s > \psi_B$	Weak inversion ($n_p>p_p$)
$\psi_s = 2\psi_B$	Onset of strong inversion ($n_p=N_A$)
$\psi_s > 2\psi_B$	Strong inversion ($n_p>N_A$)

Table 3.1: Surface potential features with different condition

3.2.2 Non-ideal MOS capacitor

In non-ideal devices, a number of charges are present in the oxide as well as at the oxide-semiconductor interface as shown in Figure 3.11. These charges are well recognised in Si technology and are known as the interface trapped charge (Q_{it}), fixed oxide charge (Q_f), oxide trapped charge (Q_{ot}) and mobile ionic charge (Q_m) [83]. The Q_{it} is due to structural defects, oxidation-induced defects, metal impurities or other defects caused by any bond-breaking process and is located at the oxide-semiconductor interface. These charges are electrically active and can be either positive or negative [12, 84]. The Q_f are mostly positive and fixed, and cannot be charged or discharged. Typically, Q_f is generated during the oxidation annealing

process and is present within a distance of approximately 3 nm of the oxide-semiconductor interface [12, 84]. The Q_{ot} is related to defects in the oxide due to the trapped electrons. In Si, generally the Q_{ot} can be mitigated by low temperature annealing (<500 °C) [12, 84]. The Q_m originate from the contamination of alkali metal ions. These charges are mobile and can diffuse in and out of the oxide under high voltage bias or high temperature which corresponds to flatband voltage shift [12, 84]. The sum of Q_f, Q_{ot} and Q_m is defined as the effective oxide charge (Q_{eff}) in the oxide [84]. These charges greatly influence the flatband voltage of MOS devices, and thus the equation 3.5 is modified by the presence of these charges and can be expressed as [12]:

$$V_{fb} = \phi_{ms} - \left(\frac{Q_f + Q_m + Q_{ot}}{C_{ox}}\right) \tag{3.27}$$

By using equation 3.27, Q_{eff} can be extracted and expressed by:

$$Q_{eff} = (\phi_{ms} - V_{fb})\, C_{ox} \tag{3.28}$$

where the density of effective oxide charge (N_{eff}) can be calculated as:

$$N_{eff} = \frac{Q_{eff}}{q} \tag{3.29}$$

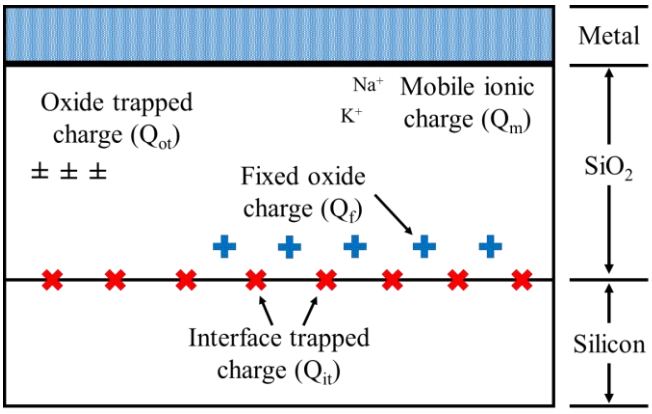


Figure 3.11: Terminology for charges in a Si MOS system

Interface traps are important features which determine the performance of 4H-SiC MOS devices. By using C-V measurement, the concentration of interface traps can be extracted utilizing the frequency response of interface states. Figure 3.12(a) shows the C-V characteristics of an ideal p-type MOS capacitor. Since the values of ϕ_{ms} and Q_{eff} are not zero, the C-V curve is shifted from the ideal curve as shown in Figure 3.12(b). Furthermore, large concentrations of Q_{it} will change the surface potential of the MOS capacitor. Then, the C-V curve is distorted and again shifted from the ideal curve as shown in Figure 3.12(c). This is due

to the fact that extra charge is needed to fill the traps, and hence it required more total charge of applied voltage to achieve the similar surface potential, ψ_s or surface band bending. This process is known as trap charge ionization and this mechanism is discussed in section 3.3.3. In addition, other than applied voltage, temperature also change the surface potential which in turn alter the C-V curve.

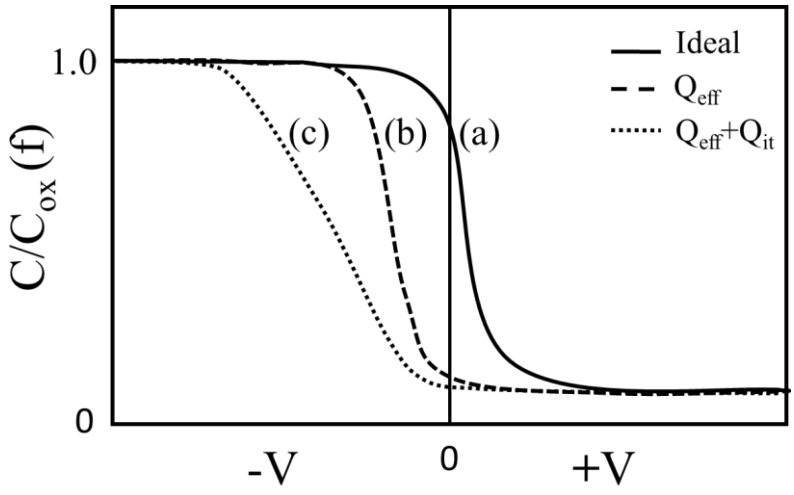


Figure 3.12: C-V characteristics of p-type MOS capacitor during accumulation: (a) ideal curve, (b) affected by effective oxide charges and (c) affected by interface trap charges

3.2.3 Metal Oxide Semiconductor Field Effect Transistor (MOSFET)

The metal oxide semiconductor field effect transistor (MOSFET) consists of a MOS capacitor with two p-n junctions. The semiconductor substrate can be either p-type or n-type and referred to n-channel and p-channel MOSFET respectively. It is a unipolar device that operates with only a single charge carrier type. The charge carrier for n-channel and p-channel are electrons and holes respectively. In this study, the n-channel MOSFET is used for explanation and discussion. A lateral conventional MOSFET is formed by four terminals which are the source, drain, gate and body as depicted in Figure 3.13. The applied voltage between the gate and source (V_{GS}) is used to create an inversion layer similar to a MOS capacitor, which controls the current flowing through the device. When V_{GS} is greater than V_{th}, an inversion channel in created underneath the oxide. However, since there is no voltage applied at the drain, there is no current conduction in the channel.

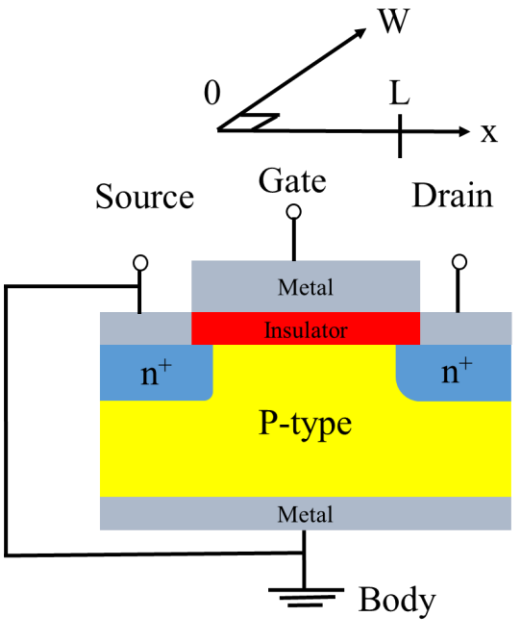


Figure 3.13: Conventional lateral MOSFET structure

When a small drain voltage (V_{DS}) is applied, a drain current (I_D) corresponding to V_{DS} starts to flow along the surface channel as shown in Figure 3.14(a). The channel voltage (V_C) is a function of x, where $V_C = V_S$ at x = 0 and $V_C = V_D$ at x = L. So, the charges in inversion channel can be expressed as [12]:

$$Q_{inv} = C_{ox}(V_{GS} - V_{th} - V_c) \tag{3.30}$$

I_D is flowing from the high voltage terminal (drain) to low voltage terminal (source) and can be expressed as [12]:

$$J_n = qn\mu_n E \tag{3.31}$$

Since the same current passes through any cross section plane, then I_D:

$$I_D = WQ_{inv}(x)\mu E \tag{3.32}$$

$$I_D = WC_{ox}(V_{GS} - V_{th} - V_c)\mu E \tag{3.33}$$

$$\int_0^L I_D\, dx = WC_{ox}\mu \int_o^{V_{DS}} (V_{GS} - V_{th} - V_c)\, dV_c \tag{3.34}$$

$$I_D = \frac{W}{L}\mu C_{ox}\left[\left(V_{GS} - V_{th} - \frac{V_{DS}}{2}\right)V_{DS}\right] \tag{3.35}$$

where μ is the electron mobility during inversion for an n-channel MOSFET, and W and L are the width and length of the channel of the MOSFET respectively. $V_{DS}^2/2$ is negligible when

small. In this region, the channel conductance (g_D) and the tranconductance (g_m) can be determined using equations 3.36 and 3.37 [12]:

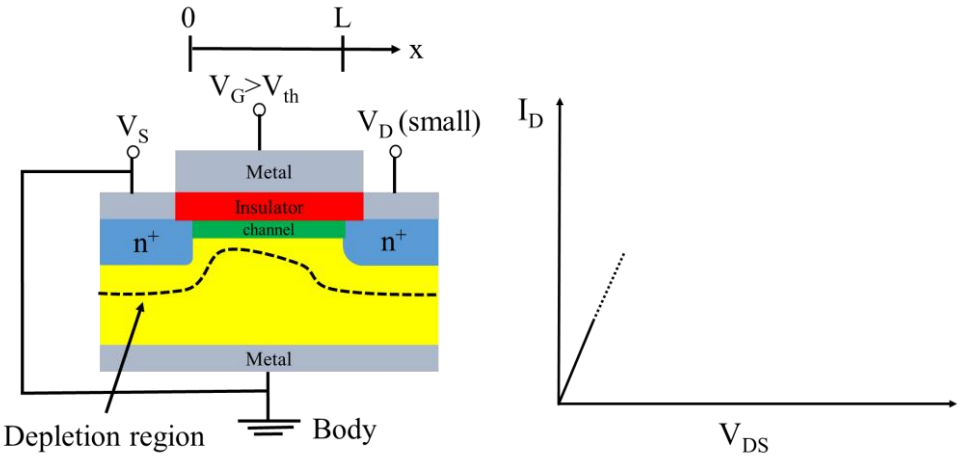
$$g_D = \frac{\partial I_D}{\partial V_{DS}}\Big|_{V_{GS}=\text{constant}} = \frac{W}{L}\mu C_{ox}(V_{GS} - V_{th}) \tag{3.36}$$

$$g_m = \frac{\partial I_D}{\partial V_{GS}}\Big|_{V_{DS}=\text{constant}} = \frac{W}{L}\mu C_{ox} V_{DS} \tag{3.37}$$

The effective mobility (μ_{eff}) and field effect mobility (μ_{FE}) are defined as follows [84]:

$$\mu_{eff} = \frac{Lg_D}{WC_{ox}(V_{GS}-V_{th})} \tag{3.38}$$

$$\mu_{FE} = \frac{Lg_m}{WC_{ox}V_{DS}} \tag{3.39}$$



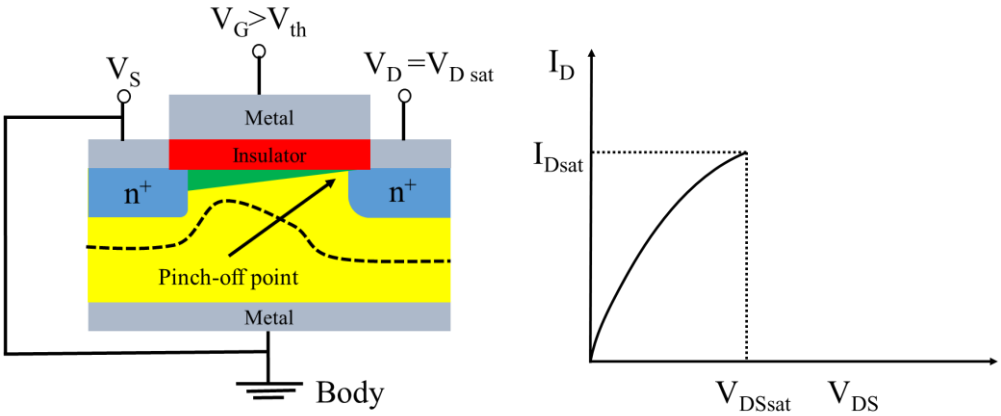
(a) (b)

Figure 3.14: (a) MOSFET operational and (b) output I_D-V_{DS} characteristics when small V_{DS} is applied

By continuing to increase V_{DS}, I_D eventually saturates and reaches the saturation value (I_{Dsat}). At this point, the I_D stops rising regardless of any further increase in of V_{DS}. In equation 3.35, $C_{ox}(V_{GS} - V_{th} - V_{DS}/2)$ can be interpreted as the average of Q_{inv} in the channel and I_D is proportional to V_{DS}. Hence, as the V_{DS} increases, Q_{inv} decreases and becomes zero. This condition is called the pinch-off, where the inversion channel is lost near the drain as depicted in Figure 3.15. Q_{inv} near to the drain can be expressed as:

$$Q_{inv} = C_{ox}(V_{GS} - V_{th} - V_{DSsat}) = 0 \tag{3.40}$$

$$V_{GS} - V_{th} = V_{DSsat} \tag{3.41}$$



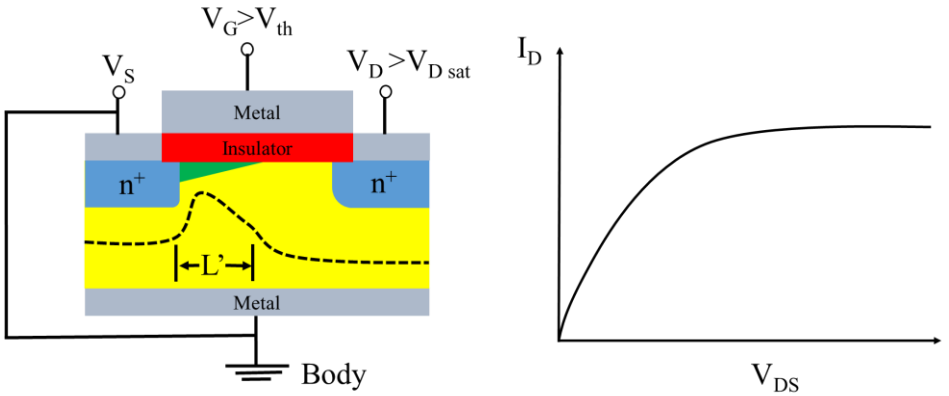
(a) (b)

Figure 3.15: MOSFET operational and output I_D-V_{DS} characteristics at the onset of I_D saturation (pinch-off point)

When a greater V_{DS} is applied ($V_{DS} > V_{DSsat}$), there is a decrease of the inversion channel length from L to L' and I_D remains constant as shown in Figure 3.16. I_{Dsat} can be obtained by substituting V_{DSsat} from equation 3.41 for V_{DS} in equation 3.35 and can be expressed as:

$$I_{Dsat} = \left(\frac{W\mu_{inv}C_{ox}}{2L}\right)(V_{GS} - V_{th})^2 \tag{3.42}$$

Beyond pinch-off, as V_{DS} increases and effective channel length decreases, the potential difference between the end of pinch-off point and drain increases and thus I_D remains constant. The voltage between the gate and source (V_{GS}) in excess of the threshold voltage (V_{th}), where V_{th} is defined as the minimum voltage required between gate and source to turn the MOSFET on, is referred to as the gate overdrive voltage (V_{GS}-V_{th}).



(a) (b)

Figure 3.16: MOSFET operational and output I_D-V_{DS} characteristics beyond I_D saturation.

3.3 Electrical Characterisation Techniques

In order to characterise the electrical features of the fabricated MOS devices, capacitance-voltage (C-V), conductance-voltage (G-V) and current-voltage (I-V) measurements were performed using an Agilent B1500A semiconductor device analyser.

3.3.1 Current–voltage measurement

In this research, all the current-voltage (C-V) measurement results were corrected for series resistance (R_s) using the series equivalent model as shown in Figure 3.17 [80, 84].

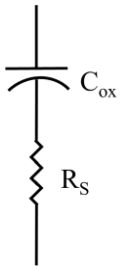


Figure 3.17: Series equivalent circuit

R_s is defined from the measured data set using equation 3.43 [80]:

$$R_s = \frac{G_m}{G_m^2 + f^2 C_m^2} \tag{3.43}$$

where G_m is the measured conductance in the accumulation region, C_m is the measured capacitance in the accumulation region and f is the measurement frequency. Then, the corrected values of conductance (G_c) and capacitance (C_c) can be calculated as given in the equations below [80]:

$$G_c = \frac{(G_m^2 + f^2 C_m^2)\alpha}{\alpha^2 + f^2 C_m^2} \tag{3.44}$$

$$C_c = \frac{(G_m^2 + f^2 C_m^2)C_m}{\alpha^2 + f^2 C_m^2} \tag{3.45}$$

where α is a variable that can be expressed as follows [80]:

$$\alpha = G_m - (G_m^2 + f^2 C_m^2)R_s \tag{3.46}$$

During strong accumulation, the values of C_{ox} is equal to the C_{max} of the device. Hence, the semiconductor dielectric constant (ε_s) or oxide thickness (t_{ox}) can be calculated using equation 3.47 [80]:

$$C_{ox} = \frac{\varepsilon_s \varepsilon_o A}{t_{ox}} \tag{3.47}$$

In addition, the V_{fb} can also be extracted directly from the C-V measurement. C_{fb} is calculated using equation 3.48 [80]:

$$C_{fb} = \frac{C_{s(fb)} . C_{ox}}{C_{s(fb)} + C_{ox}} \tag{3.48}$$

where $C_{s(fb)}$ is the semiconductor surface capacitance which can be determined by equation 3.49 [80]:

$$C_{s(fb)} = \frac{\varepsilon_s \varepsilon_o}{L_D} \tag{3.49}$$

where L_D is the Debye length which can be expressed as given in equation 3.50 [80]:

$$L_D = \sqrt{\frac{kT\varepsilon_s \varepsilon_o}{q^2 N_A}} \tag{3.50}$$

3.3.2 Split C-V technique

The capacitance can also be extracted directly from MOSFET devices using a technique for the measurement of gate-to-channel capacitance (C_{GC}) which is widely known as "split C-V" [85]. The capacitance is measured using 4 terminals of the MOSFET, including the gate, source, drain and body. The gate is connected to the applied voltage with the source and drain being a short circuit and the body connected to the ground. When $V_{GS} < V_{th}$, the surface under the gate is in the accumulation state and only the two overlap capacitances are measured as shown in Figure 3.18(a). When $V_{GS} > V_{th}$, the surface under the gate is inverted and thus the two overlap capacitance and the channel capacitance are measured as shown in Figure 3.18(b). Figure 3.18(c) shows the resulting C_{GC} from the split C-V measurement. The exact C_{ox} value during inversion is defined as in equation 3.51 [84]:

$$C_{ox} = C_{total} - C_{ov} \tag{3.51}$$

where the C_{ov} value is measured at the point where the surface begins to invert, which is near to V_{th} [84].

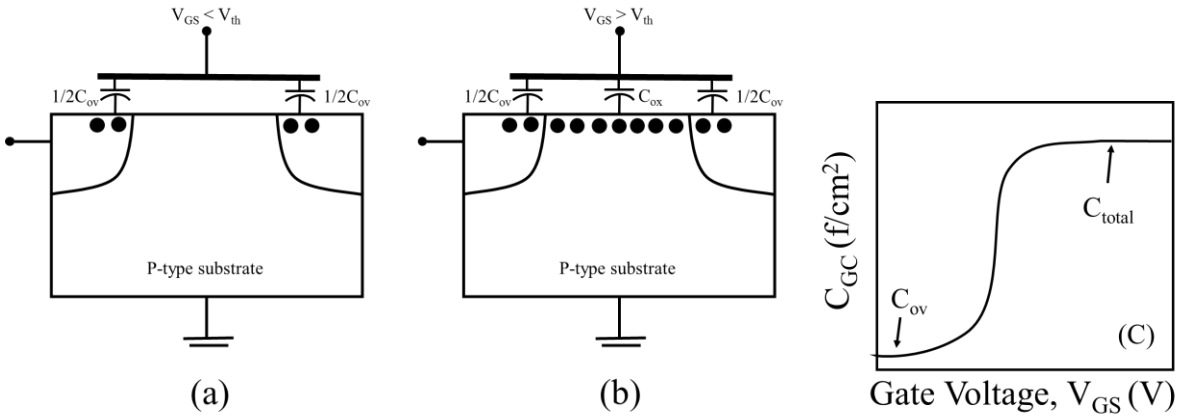


Figure 3.18: Schematic for split C-V measurements for (a) $V_{GS} < V_{th}$, and (b) $V_{GS} > V_{th}$; and (c) the resulting C_{GC} versus V_{GS} curve

3.3.3 Interface trap extraction

The Q_{it} are present at the oxide/semiconductor interface and greatly influence the performance of the MOS devices. Figure 3.19 shows the energy band diagram of the interface traps distribution during inversion of the p-type MOS system. The nature of Q_{it} are verified by experiments where the interface traps below the E_i behave as donor-like and those above E_i behave as acceptor-like [84, 86, 87]. Donor-like traps are neutral when occupied by electrons and positively charged when empty. Conversely, acceptor-like traps are negatively charged when occupied by electrons and neutral when empty. In the case of inversion of a p-type MOS, all donor-like traps are neutral and some acceptor-like traps are occupied by electrons and thus negatively charged. So according to this model, the trapped electrons at these states are almost immobile and act as Coulomb scattering centres [7]. Therefore, the acceptor-like traps near to the conduction band edge reduce the electron mobility of n-channel MOSFETs.

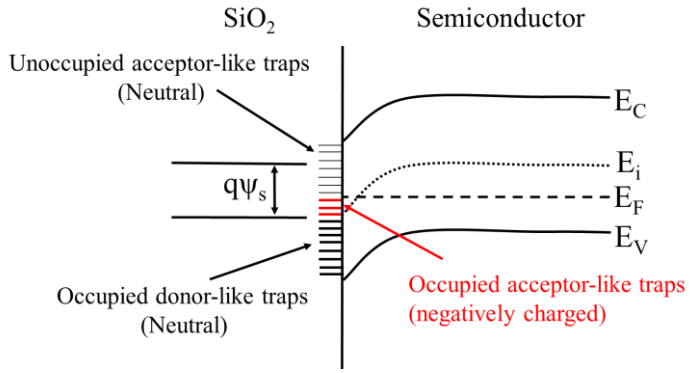


Figure 3.19: Energy band diagram illustrating the interface traps during inversion condition of p-type MOS system

The Q_{it} of the n-channel MOSFET can be determined from the C-V measurement of the n-type MOS capacitor. Figure 3.20(a) show an energy band diagram with the interface trap distribution during weak depletion of an n-type MOS system. Similar to inversion of the p-type MOS system, all donor-like traps are neutral and some of the acceptor-like traps are occupied by electrons and hence negatively charged. Q_{it} can be extracted from C-V measurement utilising the variation of frequency response. Figure 3.20(b) shows the equivalent circuit during the weak depletion state which includes interface trap capacitance (C_{it}).

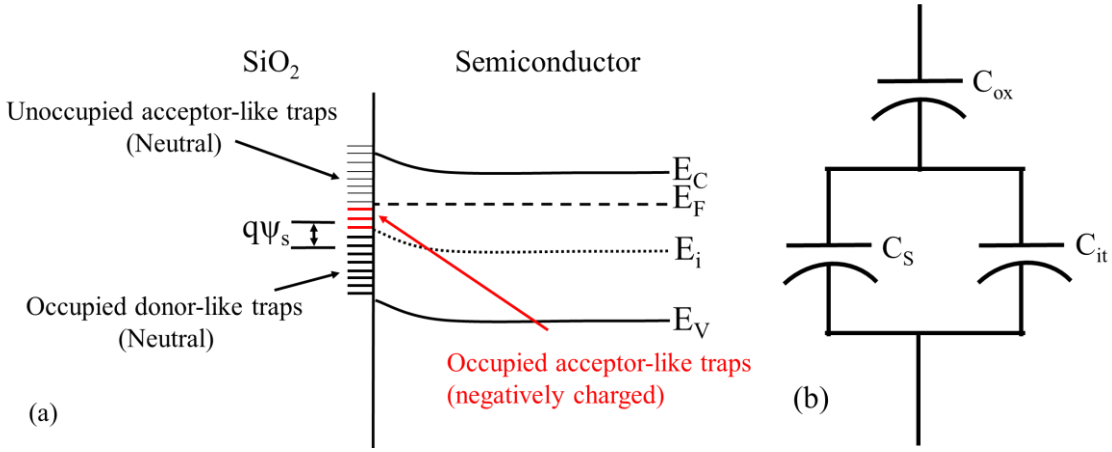


Figure 3.20: Weak depletion state of n-type MOS system; (a) Energy band diagram illustrating the interface traps and (b) Equivalent circuit consists of interface traps at weak depletion condition

In this research, Q_{it} was measured as the density of interface traps (D_{it}) using the high-low method where high and low frequency C-V measurements were performed at 1 MHz and in the quasi-static mode respectively. During these measurements, the interface trap charges are considered to fully respond during the low frequency C-V measurement. Conversely, the states did not respond to any frequency applied during the high frequency C-V measurement. From this consideration, it can be concluded that low frequency capacitance values consist of all of the interface states, while no interface traps were measured during the high-frequency C-V measurement [84]. From this assumption, the D_{it} can be calculated using equation 3.52 [84, 88]:

$$D_{it} = \frac{1}{qA}\left[\left(\frac{C_{ox}C_{lf}}{C_{ox}-C_{lf}}\right) - \left(\frac{C_{ox}C_{hf}}{C_{ox}-C_{hf}}\right)\right] \tag{3.52}$$

where A is the gate area, C_{lf} is the measured low frequency capacitance and C_{hf} is the measured high frequency capacitance. To determine the trap energy level position in the bandgap, the Berglund integral is used [89]:

$$\psi_{s(V_G)} - \psi_{s(V_{fb})} = \int_{V_{fb}}^{V_G} \left[1 - \frac{C_{lf}(V_G)}{C_{ox}}\right] \partial V_G \tag{3.53}$$

where V_{fb} is defined when ψ_s=0 V. Integrating equation 3.53 from V_{fb} to gate biases in the depletion region gives the experimental ψ_s relationship with the V_G curve. The position of the Fermi level with respect to the majority carrier band edge at the semiconductor surface is determined as a function of gate bias. The Fermi level is at a distance of $\phi_B = (kt/q) \ln (N_D/n_i)$ below the intrinsic level E_i in the bulk semiconductor. Hence, the energy position at the interface for an n-type MOS capacitor is defined as:

$$\frac{E_c - E}{q} = \frac{E_g}{2q} + \psi_s - \phi_B \tag{3.54}$$

By applying a bias V_G, ψ_s is varied and the D_{it} are scanned throughout the bandgap [80]. Then the distribution of D_{it} can be plotted as a function of energy level near to the conduction band edge. However, based on the emission time constant of the interface trap as found by Cooper *et al.* [90], the scanned energy level of the SiC MOS capacitor is limited in a range of 0.2-0.6 eV near to the valence and conduction band edge at room temperature for p-type and n-type MOS capacitors respectively. This means that interface traps located deeper than $E_c - 0.6$ eV or $E_v + 0.6$ eV are very slow and exhibit a long emission time constant (> 1 s) at room temperature and so do not contribute to the low frequency capacitance measurement [7, 90]. For an energy level shallower than $E_c - 0.2$ eV or $E_v + 0.2$ eV, the interface traps exhibit a very fast emission time constant (< 10^{-6} s) at room temperature and thus may not contribute to the low frequency capacitance measurement [7, 90].

In addition, the Terman method was also performed on the MOS devices to extract D_{it} for comparison purposes. This method only uses high frequency capacitance measurement [91]. The experimental ψ_s is extracted by comparing the measured capacitance with the theoretical value in the C-V plot. The calculated ψ_s as a function of V_G contains the interface traps and D_{it} can be extracted using equation 3.55 [80, 84]:

$$D_{it} = \frac{C_{ox}}{q^2}\left(\frac{\partial V_G}{\partial \psi_s} - 1\right) - \frac{C}{q^2} \tag{3.55}$$

3.3.4 Carrier mobility limiting mechanism

The carrier mobility in the semiconductor is limited by three major mechanisms: Coulomb scattering, phonon scattering and surface roughness scattering. The total channel mobility is given by their reciprocal sum following Matthiesen's rule:

$$\frac{1}{\mu_{total}} = \frac{1}{\mu_C} + \frac{1}{\mu_{Ph}} + \frac{1}{\mu_{Sr}} \tag{3.56}$$

where μ_C is the Coulomb scattering mobility, μ_{Ph} is the phonon scattering mobility and μ_{Sr} is surface roughness scattering mobility. The total carrier mobility is governed by the lowest scattering mobility. Takagi *et al.* [69] illustrated the schematic diagram of universal inversion layer mobility in Si MOSFETs as shown in Figure 3.21.

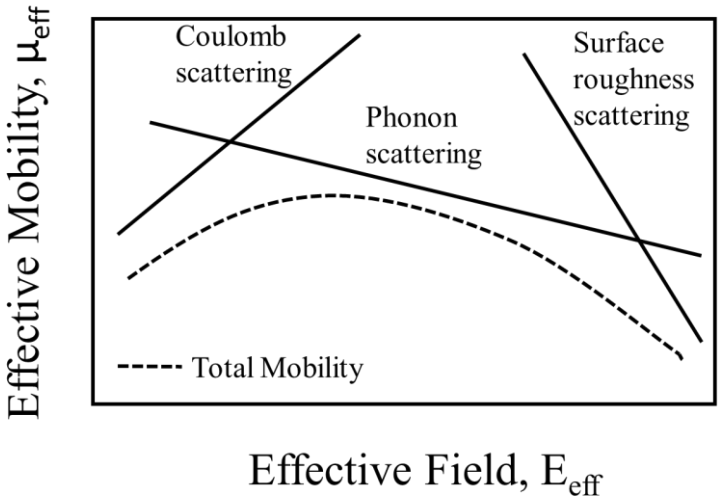


Figure 3.21: Schematic diagram of the dependence of E_{eff} on carrier mobility in the inversion layer according to the three dominant scattering mechanisms.

Each mechanism becomes the limiting factor in carrier mobility in different regions and has a particular dependency on temperature. The total mobility is also greatly dependent on the transverse effective electric field (E_{eff}) in the semiconductor that is perpendicular to the plane of the inversion channel. E_{eff} can be determined by [92]:

$$E_{eff} = \frac{1}{\varepsilon_s}\left(Q_B + \frac{1}{2}Q_N\right) \tag{3.57}$$

where ε_s is the relative permittivity in the semiconductor, Q_B is the depletion region charge density, and Q_N is the inversion carrier density. Q_B and Q_N can be described as below:

$$Q_B = \sqrt{2\varepsilon_s q N_A (2\psi_B)} \tag{3.58}$$

$$Q_N = (V_{GS} - V_{th})C_{ox} \tag{3.59}$$

Based on the universal mobility curve for Si MOSFETs, the Coulomb scattering, which originates from D_{it}, is dominant in the region of low effective electric field [69, 93]. This

Coulomb scattering mobility is inversely proportional to D_{it} and carrier concentration (N_A) but proportional to increasing temperature (T) [69]. This correlation can be expressed as:

$$\mu_C \propto \frac{1}{D_{it}} \times T \times \frac{1}{N_A} \tag{3.60}$$

As the transverse effective electric field increases, the phonon scattering mechanism starts to govern mobility in the inversion channel of the MOSFET. In this case, mobility decreases with increasing temperature and carrier concentration [69]. In order to distinguish the phonon scattering limiting factor, the temperature dependence of channel mobility is typically observed at an effective electric field of approximately 0.2 MV/cm for Si MOSFETs [69]. At this point, the contributions of Coulomb scattering and surface roughness scattering are minimal. In this region, the relationship of those factors can be expressed as follows:

$$\mu_{Ph} = \frac{1}{T} \times \frac{1}{N_A} \tag{3.61}$$

Further increases in the effective electric field squeeze the width of the inversion channel down to approximately 1 nm and hence press the carrier concentration near to the interface [93]. At this stage, inversion mobility is governed by surface roughness scattering and it rapidly decreases with effective electric field but is not affected by temperature [94]. This correlation can be modelled as:

$$\mu_{Sr} = \frac{1}{E_{eff}} \tag{3.62}$$

3.4 Structural Characterisation

Structural characterisation of the device is important in order to compare the values extracted from electrical characterisation, such as the oxide thickness and dielectric constant. In this research, the grown and deposited oxide thicknesses were measured using several methods. Atomic Force Microscopy (AFM) was used to measure a layer thickness greater than 5 nm as well as surface roughness. For a layer less than 10 nm thick, Angle Resolved X-Ray Photoelectron Spectroscopy (ARXPS) was used.

3.4.1 ARXPS measurement technique

ARXPS is a special technique used to characterise ultrathin films. The depth profile of the sample is analysed by varying its tilt angle typically in a range from 20° up to 80°. Electrons are emitted due to photon radiation from the surface of the sample. Then the electrons are detected at each of the angles before being analysed for the thickness estimation. ARXPS is

considered to be a non-destructive technique, capable of analysing films without digging down into the sample. Using this technique, a layer thickness down to the nanoscale regime can be quantitatively estimated.

Theoretically, an electron is capable of travelling a certain distance through a material before some sort of interaction occurs, and this is governed by inelastic scattering. The average distance that the electron can travel through a solid before losing energy is known as the inelastic mean free path (IMFP). During this travel, the electron experiences successive collisions so that this movement is not in a straight line.

In the ARXPS mechanism, electron emission is increased by increasing the tilt angle, thus effectively reducing the amount of information about the depth scanned as shown in Figure 3.22. Here, the detection of the electron is more sensitive to the surface. Conversely, a deeper profile of the material can be scanned when the tilt angle is decreased. By comparing the energy spectra data collected from several tilt angles, the thickness of the layer can be quantitatively estimated.

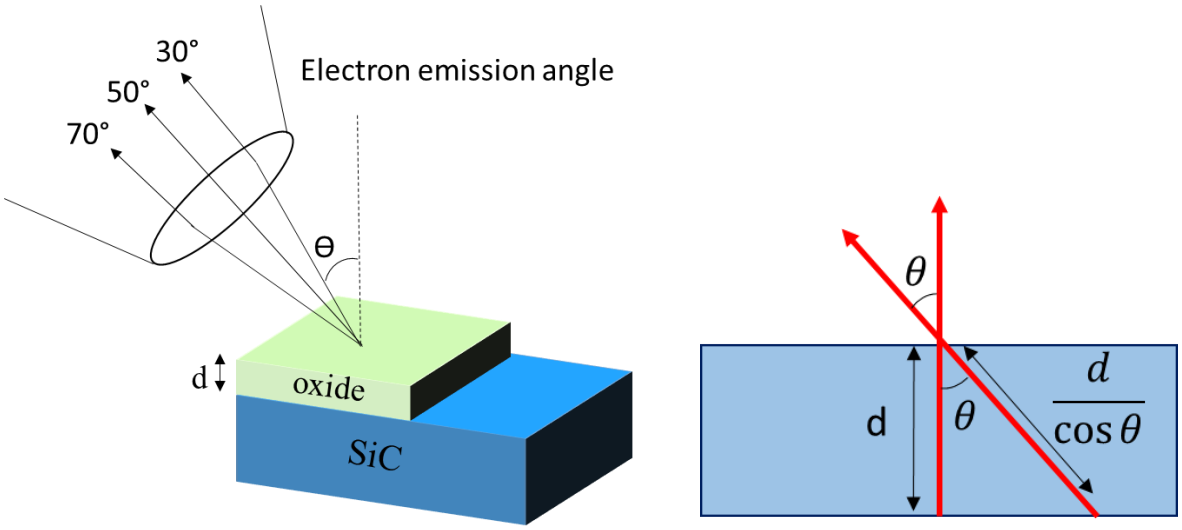


Figure 3.22: Schematic mechanism of ARXPS with different tilt angles

By using the Beer-Lambert relationship, the emitted electron intensity at an angle of 0° can be expressed by [95]:

$$I = I^{\infty} \exp\left(-\frac{d}{\lambda}\right) \tag{3.63}$$

where I^{∞} is the intensity from an infinitely thick substrate, d is the scanned depth and λ is the IMFP of the thin layer. For electrons emitted at an angle of θ to the normal, this expression becomes [96, 97]:

$$I = I^{\infty}\exp\left(-\frac{d}{\lambda\cos\theta}\right) \tag{3.64}$$

By using equation 3.64, the signal intensity from the oxide, I_{SiO_2} can be calculated by integration between from 0 to d:

$$I_{SiO_2} = \int_0^d I_{SiO_2}^{\infty}\ \exp\left(-\frac{y}{\lambda_{SiO_2(E_{SiO_2})}\cos\theta}\right)dy$$

$$I_{SiO_2} = I_{SiO_2}^{\infty}\left(1 - \exp\left(-\frac{d}{\lambda_{SiO_2(E_{SiO_2})}\cos\theta}\right)\right) \tag{3.65}$$

where E_{SiO_2}means that λ_{SiO_2}depends on the energy of the electron from the SiO_2. The signal intensity of the electron from the SiC substrate is given by the Beer-Lambert relationship:

$$I_{SiC} = I_{SiC}^{\infty}\left(\exp\left(-\frac{d}{\lambda_{SiO_2(E_{SiC})}\cos\theta}\right)\right) \tag{3.66}$$

The ratio of these signal intensities is represented as below:

$$\frac{I_{SiO_2}}{I_{SiC}} = R = R^{\infty}\frac{\left(1-\exp\left(\frac{-d}{\lambda_{SiO_2(E_{SiO_2})}\cos\theta}\right)\right)}{\exp\left(\frac{-d}{\lambda_{SiO_2(E_{SiC})}\cos\theta}\right)} \tag{3.67}$$

where $R^{\infty} = I_{SiO_2}^{\infty}/I_{SiC}^{\infty}$. The value of R^{∞} is identified by determining the areal intensity ratio of thick oxide grown on SiC with bare SiC sample. Since the electron binding energy of the electrons emitted from SiO_2 and SiC is 2p, which is approximately identical, therefore $\lambda_{SiO_2(E_{SiO_2})} \cong \lambda_{SiO_2(E_{SiC})} \rightarrow \lambda_{SiO_2}$, and the equation can be simplified as below:

$$\ln\left(1 + \frac{R}{R^{\infty}}\right) = \frac{d}{\lambda_{SiO_2}\cos\theta}$$

$$d_{SiO_2} = \ln\left(1 + \frac{R}{R^{\infty}}\right)\left(\lambda_{SiO_2}\cos\theta\right) \tag{3.68}$$

where d_{SiO_2} is the thickness of the ultrathin layer (<10 nm).

Determination of the value of λ

The value of IMFP (λ) was calculated by Tanuma *et al.* [98-100]. It depends on the kinetic energy ($E_{kinetic}$) of the electron through the material. The electron binding energy is determined by equation 3.69 based on Ernest Rutherford's 1914 work.

$$E_{binding} = E_{photon} - (E_{kinetic} + \phi) \quad (3.69)$$

where the binding energy ($E_{binding}$) is well identified, in this case, for Si-O (2p) = 102.9 eV and Si-C (2p) = 100.8 eV [101-103]. In this research, $AlK_{\alpha}X-rays$, E_{photon} = 1486.68 eV was used in the ARXPS theta probe instrument. The work function (ϕ) is an adjustable instrumental correction factor that accounts for the few eV of kinetic energy given up by the photoelectron as it becomes absorbed by the instrument's detector. In the present case, by performing calibration, ϕ is almost zero and thus is ignored. For example, the kinetic energy ($E_{kinetic}$) for SiO_2 (2p) is calculated using equation 3.69:

$$E_{kinetic} = E_{photon} - (E_{binding} + \phi)$$

$$E_{kinetic} = 1486.68\ eV - 100.2\ eV = 1386.48\ eV$$

So, based on the calculated $E_{kinetic}$ at 1386.48 eV, the value of λ calculated by Tanuma *et al.* [98-100] for an electron through SiO_2 is λ_{SiO_2} = 3.731 nm.

3.4.2 Atomic Force Microscopy (AFM)

Atomic force microscopy is a branch of scanning probe microscopy that is used to map and image features of the surface topology of samples. This scanning device can measure a wide variety of samples, including conductive and non-conductive material with comparatively low roughness. It uses a micro-machined cantilever with a sharp tip to perform sample surface measurements as shown in Figure 3.23. When the distance between the tip and the surface of the sample is relatively small, an attractive or repulsive force will be created. By utilizing this force, the deflection measured on the cantilever yields high vertical resolution information about the topology of the sample surface. From this measurement, sample contour thickness and surface roughness could be obtained for structural characterisation.

In this research, the non-contact mode was used which means that the probe tip and sample do not make any physical contact during measurement. By using this mode, an attractive Van der Waals force is utilised to record and map the sample surface topology. The accuracy of this measurement mode is down to Angstrom regime, but this value is difficult to be achieved due to the noise during the measurement. By appropriate calibration and setting, the noise can be reduced down to approximately 1 nm and allow the measurement to be performed for thickness measurement above that value. This indicates that our AFM measurement is suitable for thickness measurement above few nm.

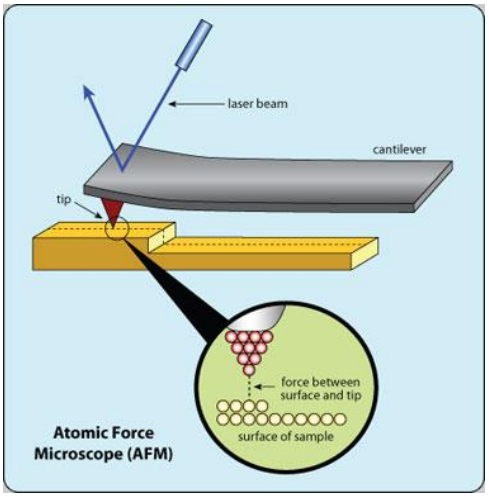


Figure 3.23: Schematic overview of the AFM concept

3.5 Device Fabrication

This section introduces the fabrication process modules used in this research. The fabrication process is discussed in detail including sample preparation, optical lithography, oxidation and metallisation.

3.5.1 Sample preparation

Before the experiments were started, all samples experienced a pre-cleaning procedure in order to remove any residual or unintended particles that could potentially degrade device performance. Initially, N-Methylpyrrolidone (NMP) and Isopropyl Alcohol (IPA) solvents were used to remove organic contaminants from the surface of the sample. The samples were immersed in NMP in an ultrasonic bath at 80 °C for 10 min. This process was repeated with IPA for 5 min and then the samples were rinsed using ultra-pure water.

Following the removal of the organic contamination, samples underwent a more rigorous organic cleaning in a mixture of Sulphuric Acid (H_2SO_4) and Hydrogen Peroxide (H_2O_2), which is also known as 'Piranha' solution. This cleaning step is essential to dissolve organic residues, particularly for hardened photoresist. A mixture of 3:1 of H_2SO_4 and H_2O_2 respectively was applied. This solution was prepared by heating up the H_2SO_4 on a hot plate before filling with H_2O_2, resulting in a "bubble like" appearance due to the chemical reaction. The samples were left on the hot plate for 10 min in order to completely remove the residual material.

Finally, the samples were cleaned using the RCA cleaning process which was developed by the Radio Corporation of America. This step could be divided into three stages:

i. Standard Cleaning 1 (SC1) : Ammonium Hydroxide (NH_4OH) and Hydrogen Peroxide (H_2O_2) were mixed in a 4:3 ratio and immersed in an ultrasonic bath at 80 °C for 10 min. This step effectively removes organic residues and particles as well as insoluble elements.

ii. Buffer Oxide Etch (BOE): A combination of Ammonium Fluoride (NH_4F), Hydrofluoric Acid (HF) and de-ionized water with percentages of 36%, 6% and 58% respectively was used. Samples were dipped into the solution for 5 s in order to remove any oxide layer and ionic residues.

iii. Standard Cleaning 2 (SC2): A combination of Hydrogen Peroxide (H_2O_2), Hydrochloric Acid (HCL) and ultra-pure water with a ratio of 3:3:2 respectively was used. In similar treatment conditions to SC1, samples were immersed in an ultrasonic bath at 80 °C for 10 min to remove remaining metallic contaminants.

Each of the above steps was followed by rinsing with ultra-pure water in order to avoid mixture combination. Finally, the cleaned samples were rinsed in ultra-pure water for 3 min and dried with a nitrogen gun.

3.5.2 Optical lithography

Optical lithography is the most important process in this study in forming the required pattern. In this research, each layer of the MOS capacitor structure was patterned via photolithography using a Karl Suss MJB-3 aligner as shown in Figure 3.24. Photolithography, which is also known as optical lithography, is an optical system that transfers a pattern from a photo-mask to a wafer using a light-sensitive chemical named a photoresist. In this research, the photoresist AZ-5214E was used. Ultraviolet light (UV) was used as a medium for image patterning exposure and it has a wavelength range between approximately 0.2 µm to 0.4 µm [1].

Figure 3.24: Karl Suss MJB-3 Aligner

Initially, the photoresist was placed on the sample before being entirely flattened using a spinner. The sample was held on the chuck by vacuum during the spinning process. In order to obtain photoresist 1.3 µm thick, the sample was spun with a rotation speed of 4200 rpm for 40 s.

There are two types of photoresist, which are positive and negative, depending on their response to light radiation. The exposed area of positive resist becomes soluble and is washed away by the developer solution (AZ 326). Thus, the remaining pattern that is formed is similar to the photo-mask. Conversely, for negative resist, the exposed area becomes polymerized and less soluble in the developer. The unexposed area is washed away and the pattern is formed in a reverse image of the photo-mask. Figure 3.25 shows an illustration of the lithography process step for both types of resists.

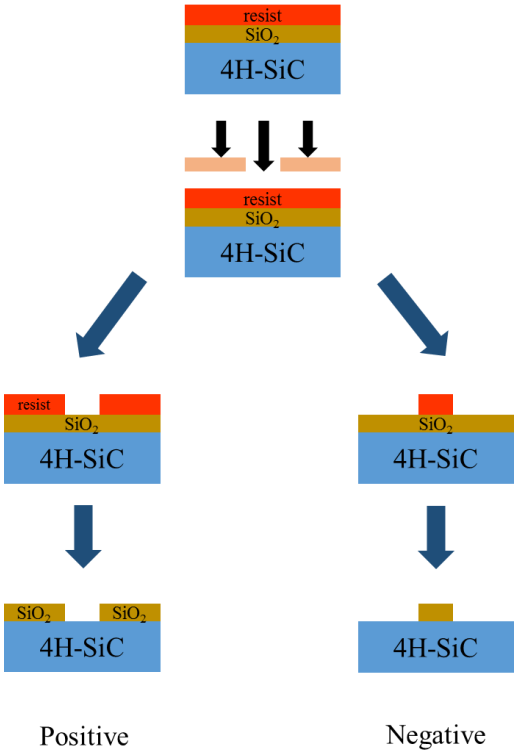


Figure 3.25: Schematic diagram of photolithographic process steps for positive and negative resists.

3.5.3 Thermal oxidation in the furnace

Thermal oxidation is a process used to form an oxide layer (SiO_2) by diffusing the oxidant species into the semiconductor surface (4H-SiC) at an elevated temperature typically in the range of 800-1200 °C in a furnace. The oxidant species reacts with the semiconductor and produces a layer of oxide in a process as in equations 3.70 and 3.71:

$$SiC + {}^{3}/_{2}\,O_2 \rightarrow SiO_2 + CO \tag{3.70}$$

$$SiC + 2O_2 \rightarrow SiO_2 + CO_2 \tag{3.71}$$

The oxidation rate can be explained using the Deal-Grove model [104] which has been accepted in the Si technology field. This model assumes an initial layer exists of SiO_2 and that oxidation occurs at the Si/SiO_2 interface, and so the process is limited by the inward movement of the oxidant rather than the outward movement of Si. The process is envisaged in Figure 3.26 and comprises the following elements:

1. A flux F_1 of oxidant species arrives at the oxide film's outer surface.
2. The oxidant is transported with a flux of F_2 across the oxide film towards the Si.
3. A flux of oxidant F_3 arrives at the Si surface and reacts to form SiO_2.

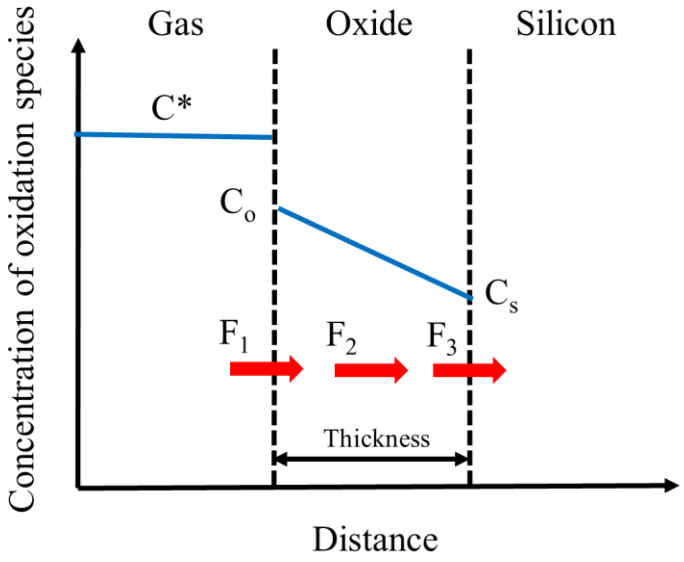


Figure 3.26: One-dimensional oxidation model

Flux equations describing each of the steps mentioned above can be written as follows [104]:

$$F_1 = h(C^* - C_o) \tag{3.72}$$

$$F_2 = D\frac{\partial C}{\partial x} = D\frac{C_o - C_s}{x_o} \tag{3.73}$$

$$F_3 = k_s C_s \tag{3.74}$$

where h is the gas-phase transport coefficient, C^* is the equilibrium concentration of the oxidant species, C_o is the concentration of the oxidants at the surface of the oxide, D is the oxidant diffusivity in the oxide, C_s is the concentration of the oxidants at the oxide/Si interface, x_o is the oxide thickness and k_s is the surface rate constant. The Deal-Grove model assume that,

under steady state conditions, all three fluxes are equal ($F_1=F_2=F_3=F$), and therefore the rate of oxide growth will be given by:

$$\frac{dx_o}{dt} = \frac{F}{N} = \frac{C^*/_N}{\frac{1}{k_s}+\frac{1}{h}+\frac{x_o}{D}} = \frac{B}{A+2x_o} \tag{3.75}$$

where N is the number of oxidant molecules per unit area, and A, B respectively are:

$$A = 2D\left(\frac{1}{k_s}+\frac{1}{h}\right) \tag{3.76}$$

$$B = 2D\frac{C^*}{N} \tag{3.77}$$

For SiC thermal oxidation, the volume of SiO_2 is equal to 2.16× the volume of SiC consumed, which is similar to the case of Si oxidation.

3.5.4 Rapid thermal processing (RTP)

Rapid thermal processing (RTP) is one of the main processes used in semiconductor manufacturing which utilises an array of lamps to heat up the sample at very rapid rates of heating and cooling. This machine can typically achieve temperatures as high as 1200 °C. Generally, RTP is used for thermal oxidation and ohmic contact formation. This process can be performed using different gas ambient or in a vacuum. In this research, RTP was used to grow the ultrathin SiO_2 layer rapidly under low temperature conditions. A ramp-up rate of 30 °C/s was used while ramp-down occurred via natural cooling. The main advantage of using RTP compared to conventional furnace methods is the ability to control the temperature and time during heating and cooling. In addition, a metal annealing process was also performed using RTP to form the ohmic contact of the devices.

Figure 3.27: RTP of JetFirst system 200C

3.5.5 Al_2O_3 deposition by Atomic Layer Deposition (ALD)

Atomic Layer Deposition (ALD) is a method of depositing dielectric materials on various substrates by utilizing a vapour phase technique. Owing to its sequential chemical process, the deposited layer thickness can be controlled to Angstrom level with excellent conformality even with structures with high aspect ratios [105]. The deposition of high k materials such as Al_2O_3 [78, 106] and SiO_2 [107] on SiC substrates have been reported. A schematic diagram of a process for depositing Al_2O_3 on 4H-SiC is shown in Figure 3.28. Initially, the 4H-SiC surface is terminated with a hydroxyl (OH) group following exposure to air as shown in Figure 3.28(a). Once the wafer has been inserted into the ALD chamber, a first chemical precursor trimethylaluminium (TMA) is introduced. The precursors react with the 4H-SiC surface but not among themselves, producing a single uniform monolayer on the surface as depicted in Figure 3.28(b). Then the TMA and any by-product elements are pumped away before introducing water vapour into the chamber as shown in Figure 3.28(c). Now the water vapour reacts with and replaces the CH_3 groups with OH groups. A further purge removes the remaining H_2O and CH_4 produced, leaving the surface terminating with OH groups as shown in Figure 3.28(d). The cycle can then be repeated to grow a film of Al_2O_3 of the desired thickness. During this process, the chamber pressure is kept at 600 mTorr with a temperature below 300 ˚C in order to prevent the surface from being oxidised. The precursors are transported to the reaction chamber by vapour draw with N_2 carrier gas. For ALD SiO_2 deposition on 4H-SiC, Yang *et al.* [107] used 3-Aminopropyltriethoxysilane, H_2O and O_3 as precursors. Figure 3.29 shows the Picosun ALD R200 ALD system that has been used in this research.

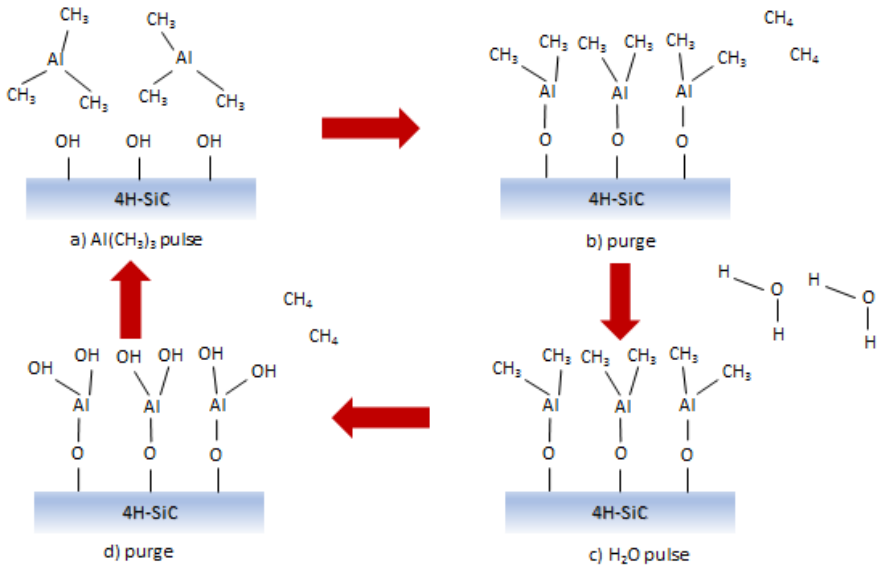


Figure 3.28: ALD reaction cycle showing the growth of Al_2O_3 using TMA and water as precursors, with CH_4 as a by-product

Figure 3.29: Image of Picosun ALD R200

3.5.6 Plasma Enhanced Chemical Vapour Deposition (PECVD)

Chemical Vapour Deposition (CVD) is the formation of a solid film on a substrate by the reaction of chemical reactants in a vapour phase that has the correct constituents. The chemical reactants are introduced into a reaction chamber at sufficient temperature to achieve decomposition and chemical reaction. Typical reactions for commonly used dielectrics in SiC technology such as SiO_2 and Si_3N_4 make use of silane (SiH_4) through the following reactions:

$$SiH_4 + O_2 \rightarrow SiO_2 + 2H_2 \quad (3.78)$$

$$3SiH_4 + 4NH_3 \rightarrow Si_3N_4 + 12H_2 \quad (3.79)$$

Unlike in conventional CVD, which relies on thermal energy to initiate and maintain chemical reactions, plasma-enhanced CVD (PECVD) uses an RF-induced glow discharge to provide energy to the reacting chemical species [108]. As a result it enables higher deposition rates at lower temperatures. Desirable properties of PECVD films include reasonable electrical parameters, good long-term reliability, good adhesion, good step coverage and conformality with underlying surfaces. A glow discharge or plasma is created by an RF field applied to a low pressure gas, which creates free electrons. These electrons gain enough energy in the applied electric field so that when they collide with reactant gas molecules, the latter are decomposed. This allows chemical reactions to take place at much lower temperatures. These energetic chemical species are then adsorbed onto the surface where a film builds up. Improved film quality compared with other CVD processes is achieved because the chemical species (radicals) form stronger bonds with the surface and can more easily migrate along it.

3.5.7 Metallisation

Metal layer deposition is required in order to connect the device structure to the outside world. In Physical Vapour Deposition (PVD), the atom from the source travels directly towards the sample. Meanwhile, in Chemical Vapour Deposition (CVD) the metal layer is formed by a chemical reaction from gases. The most commonly used methods for PVD are electron-beam evaporation and sputtering. In this research, metal and metal compounds such as Ni, Ti, Al and Al/Ti were deposited specifically for the device contact and as a mask.

In the e-beam evaporation technique, samples were placed in a vacuum chamber with low pressure down to approximately 10^{-6} mbar. The target material was bombarded using an electron beam gun and metal atoms are emitted. Then the ejected atoms are focused by a magnetic field to travel towards the samples as shown in Figure 3.30. During this process, low pressure conditions are required in order to reduce collisions between ejected metal atoms and gas molecules.

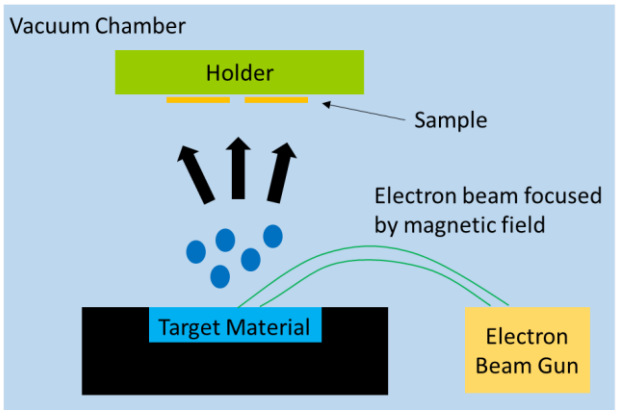


Figure 3.30: Schematic of electron-beam evaporation process

Similar to the evaporation method, sputtering is also performed in a vacuum chamber. The samples were placed opposite to parallel plates with the target material as shown in Figure 3.31. An inert gas such as Ar was inserted into the chamber and transformed into positive Ar^+ by plasma. The surface of the metal target, which was maintained at a negative potential, was then bombarded by energetic particles of Ar^+ initiating source atoms to be ejected from the atomic bonding. Being neutral, the ejected atoms then travel to the sample and form the required thin film.

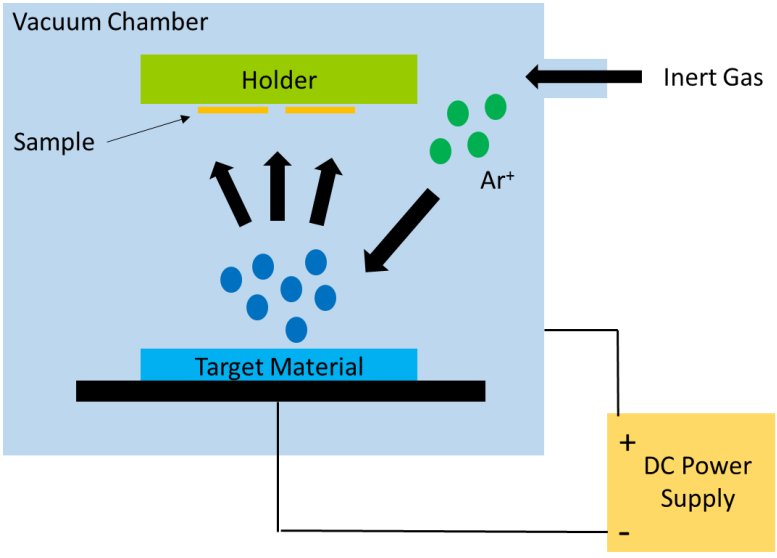


Figure 3.31: Schematic of DC sputtering process

3.6 Summary

This chapter has discussed the fundamentals, characterisation techniques and fabrication processes used in this research. Initially, the basic characteristics of the MOS devices with different working modes have been described. Then, the electrical and structural

characterisation that was performed on the fabricated devices has also been presented. The C-V measurement technique, including series resistance correction, the split C-V technique and interface trap extraction, have been introduced. Furthermore, the channel mobility limiting factors in MOSFETs have been explained. Then, a detailed explanation was given of the structural characterisation of fabricated devices using ARXPS and AFM. This measurement is important, since accurate values of the thickness of the grown SiO_2 are needed, which is one of the key results in this research.

Most of the fabrication process modules which were employed in this research have also been discussed. Several oxide formation processes have been explained, including thermal oxidation in the furnace, rapid thermal processing, atomic layer deposition and plasma-enhanced chemical vapour deposition.

Chapter 4

4H-SiC MOS Capacitor Using Ultrathin SiO_2/Al_2O_3 Gate Stack

4.1 Introduction

The Metal Oxide Semiconductor (MOS) capacitor is one of the most important structures in semiconductor physics because it is a key component for Field Effect Transistors (FET) devices. Sze and Ng [12] have described the MOS capacitor as the "heart" of the MOSFET, which is the most important device in advanced integrated circuits (ICs). Basically, the MOS capacitor is formed by growing or depositing oxide on the semiconductor surface followed by metal deposition. The oxidation process is the critical step that defines the quality of grown oxide and the interface between oxide and semiconductor which determines the performance of the MOS device. In silicon (Si) based technology, silicon dioxide (SiO_2) is thermally grown on Si at a temperature around 1000 °C followed by low temperature hydrogen (H_2) annealing at 450 °C. The annealing process effectively passivates the trapped charge defects at the interface which is the main cause of limiting the electron mobility [12]. The density of interface traps (D_{it}) is reduced as low as 10^{10} $cm^{-2}\cdot eV^{-1}$, which is sufficient to operate MOS and MOSFET devices efficiently [12]. This technique is widely used in the manufacturing of Si electronic devices [109]. However, in the case of silicon carbide (SiC), and particularly 4H-SiC, the problem of poor interface quality, which is mainly due to high values of D_{it}, is still not resolved even though extensive research has been carried out [7]. Typically, researchers have tried to implement a fabrication technique similar to that of Si technology, for example

using oxidation and passivation processes at high temperature in H_2 [72], nitridation [36, 37, 42, 43], Argon (Ar) [76] and etc. However, these methods do not work with 4H-SiC devices.

With Si technology, only Si and oxygen (O) take part in the chemical reaction giving rise to the growth of SiO_2. However, the thermal oxidation of 4H-SiC substrates, carbon (C) atoms react with O and form different molecules. Theoretically, C atoms are released during the thermal oxidation of 4H-SiC as CO or CO_2 gases. However, a small fraction of C atoms do not react with O. These C atoms are trapped inside the 4H-SiC bulk near to the 4H-SiC/SiO_2 interface and are believed to be the cause of high concentrations of interface traps that cause the performance of 4H-SiC MOS capacitors to deteriorate [33, 110-113].

Recently, Shen and Pantelides [33] proposed that thermally grown oxide leaves C atoms as single interstitials, (C_i) inside the 4H-SiC substrate. These excess C atoms combine with each other and generate a large concentration of C clusters named C di-interstitials, $(C_i)_2$ chains. This $(C_i)_2$ is physically immobile and can retain its position even with surface treatment, and therefore it becomes a major factor in high concentrations of interface traps at the SiO_2/4H-SiC interface. A massive concentration of $(C_i)_2$ inside the 4H-SiC substrate is believed to have been detected after thermal oxidation using Deep Level Transient Spectroscopy (DLTS) [114], Raman spectroscopy [26] and Electron Energy Loss Spectroscopy (EELS) [25]. As a consequence, thermal oxidation produces high values of D_{it} at the interface, leading to poor channel electron mobility in 4H-SiC MOSFETs, typically below 10 $cm^2/V.s$ [36, 37].

This chapter describes the fabrication of p-type and n-type 4H-SiC MOS capacitors in an investigation of the quality of the grown oxide and especially its interface with 4H-SiC. The oxide was grown using a low thermal budget in order to generate less C related defects and to further reduce the values of D_{it} which compromise device performance. Alongside low thermal budget devices, control devices having higher temperature oxidation at 1150 °C were also fabricated. Details of the fabrication processes used in both methods are fully described. The results of physical and electrical characterisation of the fabricated devices are then presented. The electrical stability of the device at high temperatures as well as gate oxide robustness are also investigated.

4.2 Experimental Details

4.2.1 Low thermal budget technique

P-type MOS capacitors with heavily doped n-type substrate were fabricated on 3.84° off-axis (0001) Si face, n^+ (sub)/p^+ (10^{17} cm^{-3}, 5 µm)/p^- (6.7×10^{15} cm^{-3}, 1 µm) epitaxial 4H-SiC (0001) wafers supplied by Cree. Firstly, the samples were cleaned with Piranha solution followed by the standard Radio Company of America (RCA) cleaning procedure. The cleaning process details are described in section 3.5.1. Photoresist depositions for the photolithography processes were carried out in an EMS 6000 photo resist spinner, using AZ 5214E photoresist at a spin velocity of 4000 rpm for 40 s, resulting in a photoresist thickness of 1.3 µm. Then, the photoresist was patterned using a Karl Suss MJB-3 Aligner and the designated mask, and this step was performed in every lithography step. The fabrication steps for p-type MOS capacitors were carried out as follow:

- Definition of the mesa structure: Mesa structures were created for every device for electrical isolation. A Mesa Mask (Table 4.1-1) was used to pattern the photoresist before 7 nm of Titanium (Ti) as the adhesion layer and 120 nm of Nickel (Ni) were deposited using BOC-Edwards auto e-beam evaporators as the etching mask. The metal was lifted-off using N-Methyl-2-pyrrolidone (NMP) for 3 min in ultrasonic bath following by Isopropanol (IPA) cleaning. Next, the samples were etched using the Plasma Therm 790 Reactive Ion Etching (RIE) process. This process was performed for 80 min in order to completely etch to a 5 µm depth. The remaining metal was then removed by dipping in Aluminium (Al) etchant for 30 min in the ultrasonic bath followed by 2 min of a buffered oxide etch (BOE) dip.
- P^- epi-layer etching: The PPLUS Mask (Table 4.1-2) was patterned on the photoresist and similar processes as above were repeated with a metal deposition of 7 nm Ti and 50 nm Ni as a mask for a 1 µm 4H-SiC etch. This etching process was performed to open a contact on the doped p^+ epilayer ($N_A = 1 \times 10^{17}$ cm^{-3}). Then the metal removal process using Al etchant and BOE was undertaken. After this stage, the following steps vary depending on the type of oxide to be grown.

  In the typical thermal oxidation technique for MOS fabrication, the contact formation with metal deposition and metal annealing were performed after oxide growth as the last step. In such case, the oxide may be exposed to a high temperature during the metal annealing process. This will produce an additional SiO_2 layer and generate more C defects which will adversely affect the performance of the device.

Unlike the standard thermal oxidation technique, the thermal budget technique requires modifications in order to protect the 4H-SiC surface from exposure to higher temperatures. Figure 4.1 illustrates the modification of the process in order to achieve a low thermal budget gate oxide.

- Metal contact formation: Next, after the etching process, samples were patterned by using the Metal 1 Mask (Table 4.1-3). Then, a stack of metal consisting of 5 nm Ti / 45 nm Al / 15 nm Ti / 45 nm Al / 10 nm Ti was evaporated by e-beam to form metal-semiconductor contacts. After the lift-off process, post metallisation annealing (PMA) was performed at 1000 °C for 3 min in a high vacuum chamber using Jet First 200 Rapid Thermal Processing (RTP). A chamber pressure of 7×10^{-4} mbar was recorded during this annealing. This step is necessary in order to produce stable ohmic contact behaviour [115]. Then, a 100 nm Si_3N_4 layer was deposited at 220 °C using Plasma Enhanced Chemical Vapour Deposition (PECVD). This layer is used to protect the metal contact during the subsequent oxidation process and also to create an additional isolation layer between the oxide gate and metal contact [116].
- Gate oxide formation: Then samples were patterned using a Dielectric Mask (Table 4.1-4) before the Si_3N_4 layer was etched over the gate area using BOE for 1 min, where photoresist was used as a mask for this etching. After the etching and the removal of the photoresist, the samples were oxidised using RTP at several low temperatures for a short duration. The thicknesses of these SiO_2 layers were determined by Angle Resolved X-Ray Photoelectron Spectroscopy (ARXPS) compared to control samples oxidised alongside. Then the gate insulator stack was completed with the deposition of 40 nm of aluminium oxide (Al_2O_3) by Atomic Layer Deposition (ALD) immediately after oxidation. Adduct-grade trimethylaluminium (TMA) and H_2O were used as precursors and were transported to the reaction chamber in vapour draw with a nitrogen (N_2) carrier gas. Deposition was performed at 200 °C at a chamber pressure of 600mTorr with pulse/purge lengths of 0.1/4 s for TMA and 0.1/6 s for H_2O respectively.
- Gate electrode formation: Next, the samples were patterned with the Metal 2 Mask (Table 4.1-5) before gate contact was formed by the deposition of 150 nm Al. The devices were completed with a contact opening in the Si_3N_4 layer with RIE using photoresist as a mask as depicted in Figure 4.2. Figure 4.3 shows a microscopic image of the fabricated p-type MOS capacitors using the low thermal budget technique.

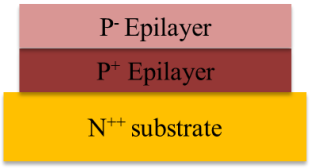
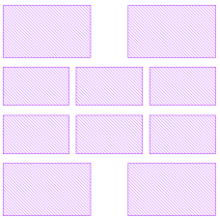
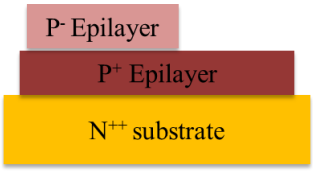
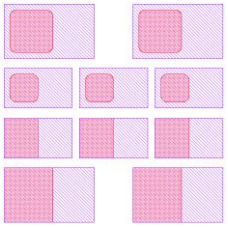
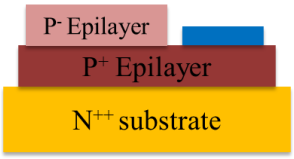
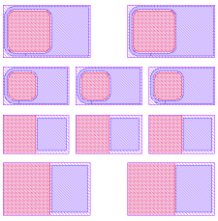
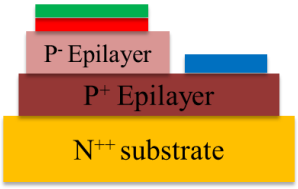
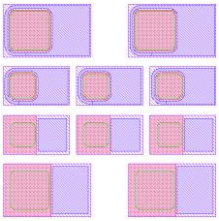
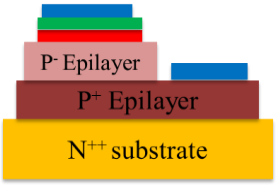
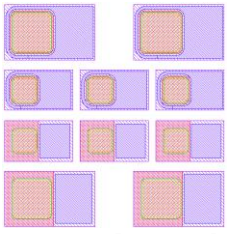
Cross Sectional View	Mask Set
 1) Mesa structure	 Mesa Mask
 2) PPLUS etch	 PPLUS Mask
 3) Metal contact deposition and annealing	 Metal 1 Mask
 4) Oxidation and Al_2O_3 deposition	 Dielectric Mask
 Gate contact metallisation	 Metal 2 Mask

Table 4.1: Fabrication steps with mask configuration of low thermal budget MOS capacitor

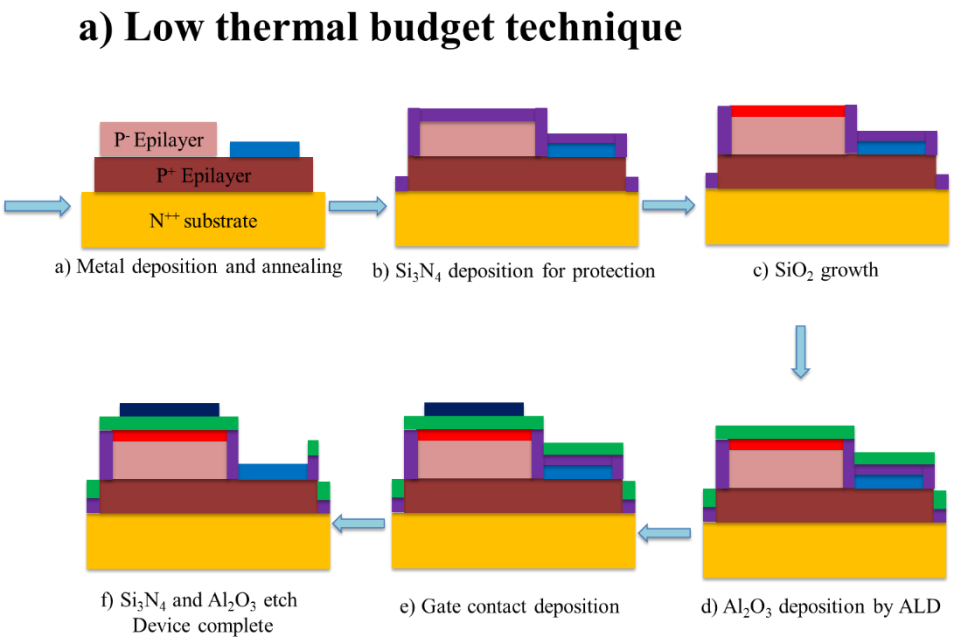


Figure 4.1: MOS fabrication process with a) low thermal budget technique and b) standard thermal oxidation technique

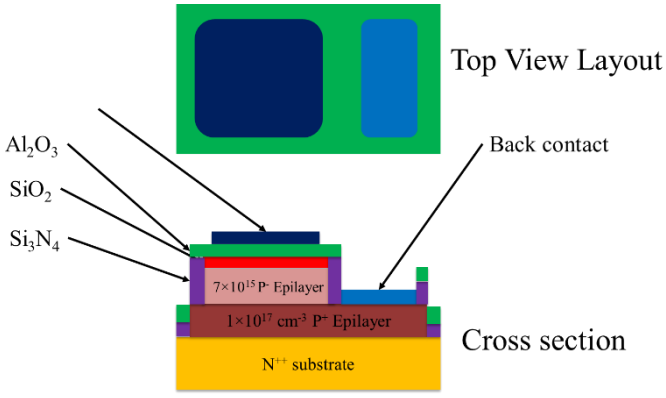


Figure 4.2: Schematic top view and cross section of fabricated p-type MOS structure

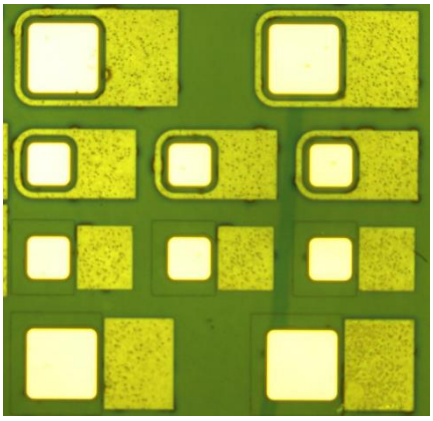


Figure 4.3: Microscopic image of fabricated p-type MOS capacitors using low thermal budget technique

4.2.2 1150 ℃ oxidation technique

For the control MOS capacitor, a surface preparation process was performed before the gate oxide growth to fully treat the surface. The sacrificial oxide was oxidised at 1150 °C for 60 min in dry O_2 ambient in the furnace. Then, this oxide layer was removed by wet etching using BOE for 30 s to produce the renewed 4H-SiC surface. Then, the critical step to produce gate oxide followed. The samples were oxidised at 1150 °C for 180 min in an O_2 flow rate of 150 sccm in the furnace, resulting in a SiO_2 layer of 28 nm thick. This gate oxide was then covered by photoresist, allowing the metallisation of the back contacts. To form metal back contacts, a similar stack of metal consisting of Al and Ti was evaporated using the e-beam evaporator, followed by PMA using RTP at 1000 °C for 3 min. Finally, the devices were completed with the deposition of 100 nm Al to form the gate contacts.

4.2.3 N-type MOS capacitor fabrication process.

In addition to the p-type MOS capacitor, n-type MOS capacitors were also fabricated on epitaxial 4H-SiC wafers (7.83° off-axis, Si-face, n^+ (sub)/n^+ (10^{18} cm^{-3}, 1 μm)/n^- (8.72×10^{14} cm^{-3}, 45 μm) supplied by Cree. Unlike the p-type MOS capacitor where a lateral structure was used, the n-type MOS capacitors were fabricated with vertical geometry as depicted in Figure 4.4. After cleaning using the RCA procedure, the top surfaces of the samples were covered with photoresist and they were baked at 150 °C for 15 min followed by 130 °C for 15 min. This step hardens the photoresist to avoid it being etched by the BOE dip before back contact metallisation. Then 5 nm of Ti and 100 nm of Ni were evaporated onto the bottom side of the sample using the e-beam evaporator [117]. High vacuum annealing at 1000 °C for 3 min was performed using RTP in order to achieve ohmic contact. During this process, a chamber

pressure of approximately 7×10^{-4} mbar was applied after pumping down the chamber for 120 min. To protect the metal contact at the bottom side from being oxidised, 100 nm of Si_3N_4 was deposited at 220 °C by PECVD. After that, the samples were dipped in a BOE before immediately being oxidised in RTP using the low thermal budget technique to produce an ultrathin layer of SiO_2. To complete the gate stack, a 40 nm layer of Al_2O_3 was deposited by ALD using a similar recipe to that for p-type MOS capacitors. Next, the samples were patterned and 100 nm Al was deposited on top as a metal gate using the e-beam evaporator. Finally, the top side of the sample was covered by baked photoresist in order to etch the Si_3N_4 layer by RIE. For the higher temperature technique, the steps of the process are in the reverse order, where the gate oxide was grown before the metal back contact formation as the final step. Post oxidation annealing in N_2O was performed on certain samples at 1150 °C for 70 min in the furnace. Neither Si_3N_4 nor Al_2O_3 deposition were involved in this gate oxide process.

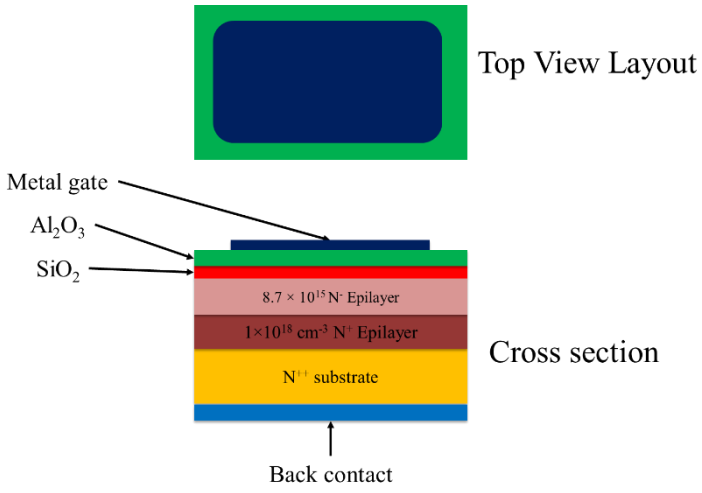


Figure 4.4: Schematic top view and cross section of fabricated n-type MOS structure

4.3 Device Characterisation Results

In this research, Atomic Force Microscopy (AFM) and Angle Resolved X-Ray Photoelectron Spectroscopy (ARXPS) characterisation techniques were used to determine physical structure. Layers of a thickness above 5 nm were measured efficiently using the non-contact mode of AFM. For layer thicknesses less than 10 nm or in the sub-nanometer regime, the ARXPS technique was employed. Details of both methods are explained in sections 3.4. It is necessary to determine the physical thickness of grown SiO_2 and deposited Al_2O_3 in order to compare results with the effective oxide thicknesses (EOT) obtained from electrical characterisation.

For electrical characterisation, an Agilent B1500A semiconductor device analyser has been used. I-V, C-V and G-V measurements have been performed to determine device performance.

4.3.1 Ultrathin oxide growth

Oxide growth condition were varied in order to investigate the dependence of D_{it} on oxide thickness. Samples were oxidised at several times in the range of 1–5 min with different growth temperatures from 600 °C to 800 °C using RTP. In order to determine the thickness of the ultrathin SiO_2 layer, ARXPS was used. Energy spectra in the range of Si-O and Si-C 2p bonding energy with different take-off photoelectron emission angles of 30°, 50° and 70° were measured to estimate the oxide layer thickness. Figure 4.5 shows the ARXPS results with a take-off angle of 70° for devices fabricated with oxide growth at 600 °C for 1-3 min. Data for bare 4H-SiC was also plotted as a control. Small peaks of Si 2p that appeared at a binding energy of 102.9 eV verify the existence of an ultrathin SiO_2 layer [101, 118]. A slight peak increase with increasing oxidation time from 1 to 3 min was observed which corresponds to the SiO_2 layer thickness. The areal ratio of SiO_2 and 4H-SiC intensities were used to estimate oxide thicknesses as explained in section 3.4.1 [96, 98-100]. Table 4.2 shows the SiO_2 layer thicknesses resulting from different oxidation times, and the results provide evidence that an ultrathin layer of oxide has been successfully grown in the nanoscale regime.

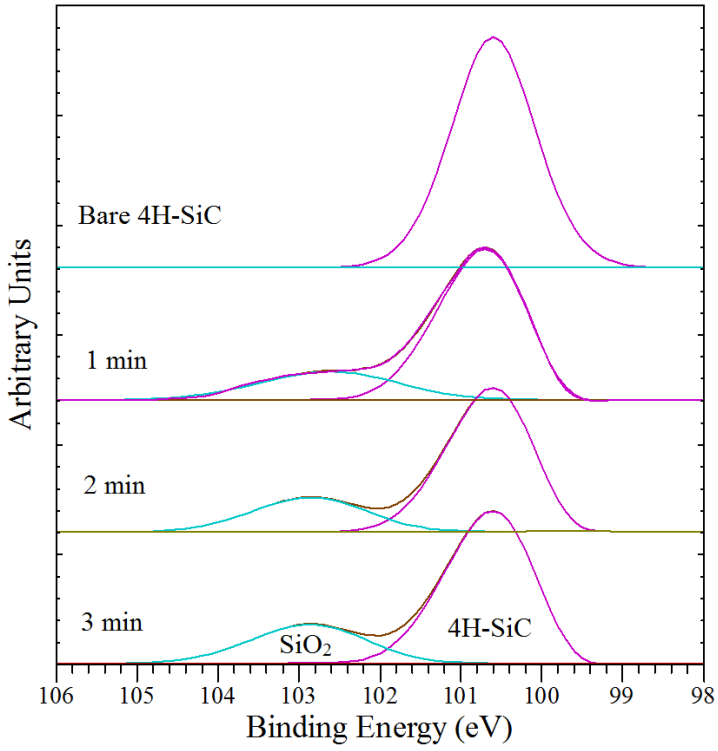


Figure 4.5: ARXPS results for oxide growth at 600 °C for 3 min with take-off angle of 70°

Oxidation time (min)	SiO_2 thickness (nm)
1	0.58
2	0.63
3	0.71

Table 4.2: Ultrathin SiO_2 thickness results at 600 °C

4.3.2 High-k dielectric of Al_2O_3 deposition by Atomic Layer Deposition (ALD)

Dielectric Al_2O_3 was deposited using ALD over the grown ultrathin oxide layer to complete the gate stack. The AFM technique was used to determine the thickness of the Al_2O_3 layer as shown in Figure 4.6. This high-k dielectric material also serves as an extra passivation layer to avoid leakage current while offering high capacitance. Verification of the exact Al_2O_3 layer thickness is necessary in order to determine the effective oxide capacitance (C_{ox}) of the MOS capacitor from capacitance-voltage (C-V) measurements during the accumulation stage.

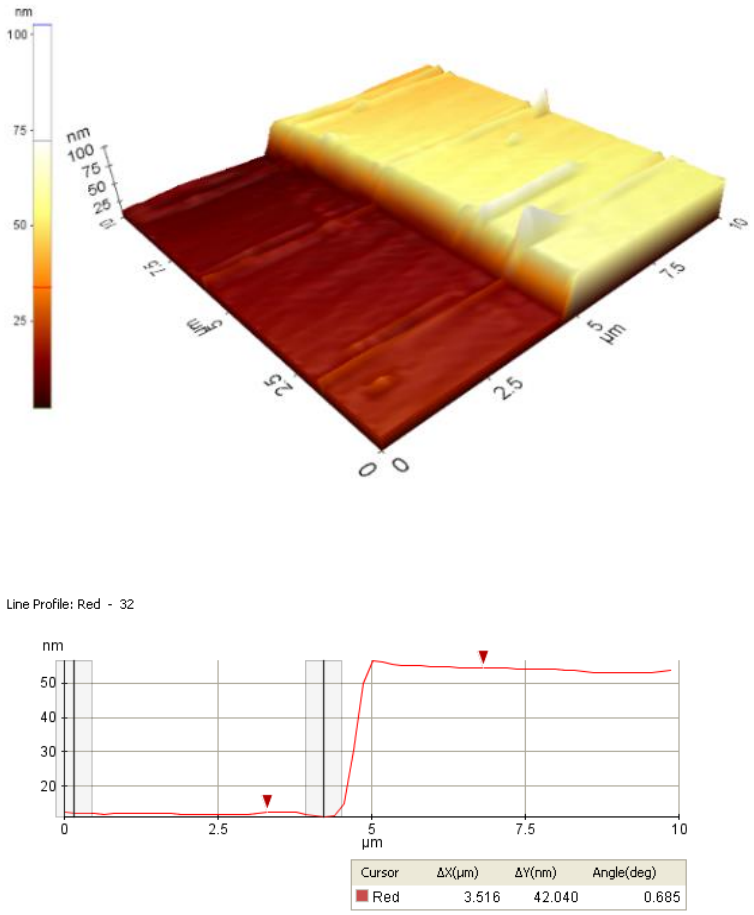


Figure 4.6: AFM images of Al_2O_3 layer deposited by ALD

4.3.3 Specific contact resistivity, ρ_c on p-type 4H-SiC

A metal-semiconductor (MS) contact connects the semiconductor with outside metal circuitry. This structure is required in all semiconductor devices to pass current into and out of the device. The MS contact can be either rectifying (Schottky) or non-rectifying (ohmic). Since SiC is a wide bandgap material, it is difficult to find a contact metal which has a low barrier height. Figure 4.7 demonstrates the 4H-SiC band diagram with electron affinity, χ_s of about 3.6 eV [113] and a bandgap 3.26 eV at room temperature. Ideally, a metal contact with a work function lower than 4 eV will work perfectly as an ohmic contact for n-type 4H-SiC, whereas the work function should be above 7 eV for a p-type 4H-SiC. However in reality, it is difficult to find a metal with such a large value of work function, particularly for the p-type 4H-SiC, which thus will form a good ohmic contact.

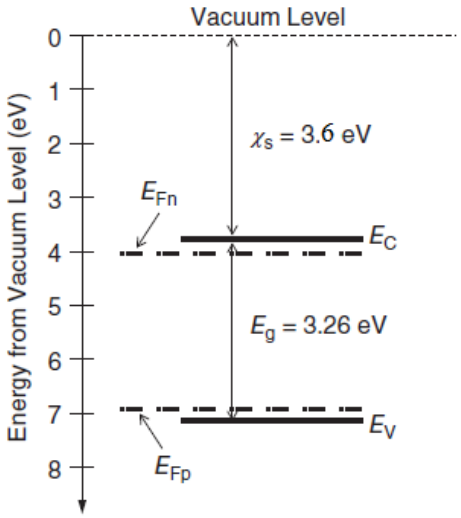


Figure 4.7: 4H-SiC band diagram including vacuum level [119].

Most of the metals deposited on 4H-SiC act as Schottky contacts, unless metal annealing at a temperature above 700 °C is performed or the 4H-SiC material is highly doped [7]. In this research, a good ohmic contact that shows low specific contact resistivity (ρ_c) is required so as to connect the device to a measurement probe without any voltage drop. The contact resistivity should be negligibly small (<1%) compared to the device resistance [7]. For n-type 4H-SiC, an alloy consisting of Ni/Ti is typically used where ρ_c as low as ~ 10^{-5} – 10^{-6} $\Omega.cm^2$ was found. [7].

On the other hand, extensive studies are still ongoing to find a metal or alloy that could form a good ohmic contact for the p-type 4H-SiC. Crofton *et al.* [120] obtained values of ρ_c as low as $1.7 \times 10^{-3}\ \Omega.cm^2$ for a p-doping concentration of $1 \times 10^{17}\ cm^{-3}$ using deposited Al/Ti on 6H-SiC, as shown in Figure 4.8. This deposited alloy experienced PMA at 1000 °C for 5 min in Ar. Note that the values of bandgap and electron affinity for 6H-SiC are 3.02 eV and 3.85 eV respectively and hence it has almost similar work function values than that of 4H-SiC [119]. Figure 4.8 also demonstrates that values of ρ_c less than $1 \times 10^{-5}\ \Omega.cm^2$ can only be achieved at the higher doping level of $3 \times 10^{19}\ cm^{-3}$. Hyung *et al.* [121] reported that a ρ_c of $1.9 \times 10^{-3}\ \Omega.cm^2$ was achieved at a doping concentration of $4 \times 10^{17}\ cm^{-3}$ using Ni/Ti/Al deposited on 4H-SiC. The metal contacts were annealed at 800 °C for 2 min in Ar ambient. To date, only two studies [120, 121] have reported values of ρ_c for doping concentrations at about $10^{17}\ cm^{-3}$ for p-type epitaxial 4H-SiC.

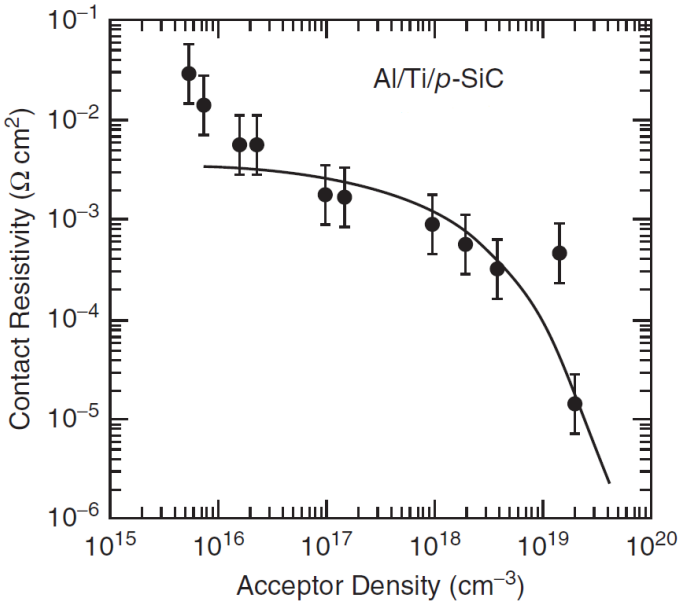


Figure 4.8: Contact resistivity of Al/Ti over acceptor density of epitaxial 6H-SiC [120].

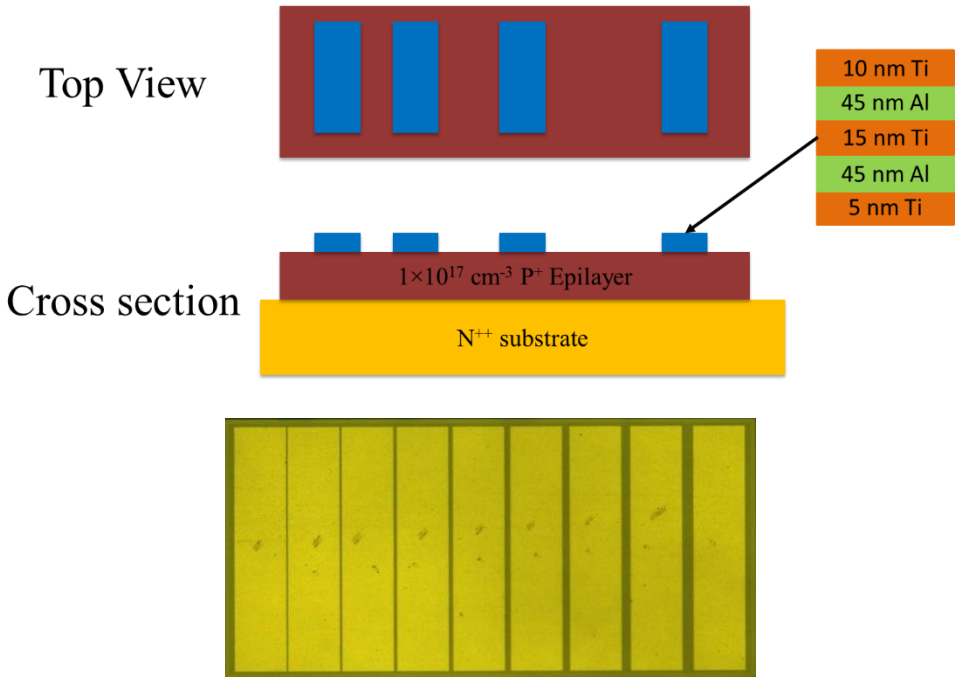


Figure 4.9: Schematic top view and cross section (above) and fabricated TLM structure with a stack of metal (Al/Ti) (below).

In order to fabricate p-type MOS capacitors, it is important to obtain a good ohmic contact on p-type 4H-SiC with a doping level of 1×10^{17} cm^{-3}. A stack of metal consisting of 5 nm Ti, 45 nm Al, 15 nm Ti, 45 nm Al and 10 nm Ti was deposited by e-beam evaporator to form the metal contact. Such a proportion was used in order to uniformly mix the alloy with an Al/Ti weight ratio of 2:1. After that, PMA was performed in a high vacuum and forming gas ambient at 1000 °C for 3 min using RTP. For the high vacuum annealing process, the chamber was pumped down for 120 min to achieve a pressure of approximately 1.7×10^{-5} mbar before the temperature was increased up to 1000 °C. During the annealing process for 3 min, the chamber pressure increased to 7.0×10^{-4} mbar. On the other hand, forming gas which contains a mixture of H_2 and N_2 was purged into the chamber during the annealing process.

The value of specific contact resistance was calculated using the transfer length method (TLM). The TLM structure consists of a metal stack fabricated over the mesa structure to minimize current flow lines from the top and bottom of the contacts. Figure 4.9 shows the fabricated TLM structure which were made of 9 pads with different spacing varying from 20 to 140 µm. Each pad has a length of 100 µm and width of 250 µm. Figure 4.10 shows the total resistance as a function of contact pad spacing in a range of 20 to 140 µm for both processes. The value of ρ_c can be obtained from the line intercept [84]. Values of ρ_c as low as 1.5×10^{-3} $\Omega.cm^2$ were obtained for the high vacuum annealing as shown in Figure 4.11. This suggests

that no interaction occurred between the gas molecules and metal contact, which enabled a clean metal stack annealing process. For comparison, this value is in agreement with the results of Crofton *et al.* [120] where Ar gas was used. On the other hand, a value ρ_c of 1.5 $\times 10^{-2}$ $\Omega.cm^2$ was found when forming gas was used. This is an increase of one order of magnitude compared to the value for metal contacts annealed in high vacuum ambient. Theoretically, the forming gas reduces the oxide during the annealing process. However, there is the possibility of gas molecules reacting with the metal contacts and thereby increasing the ρ_c value. Each point of the ρ_c value is the average from 5 different devices. (It should be noted that Ar gas is not available in our RTP.)

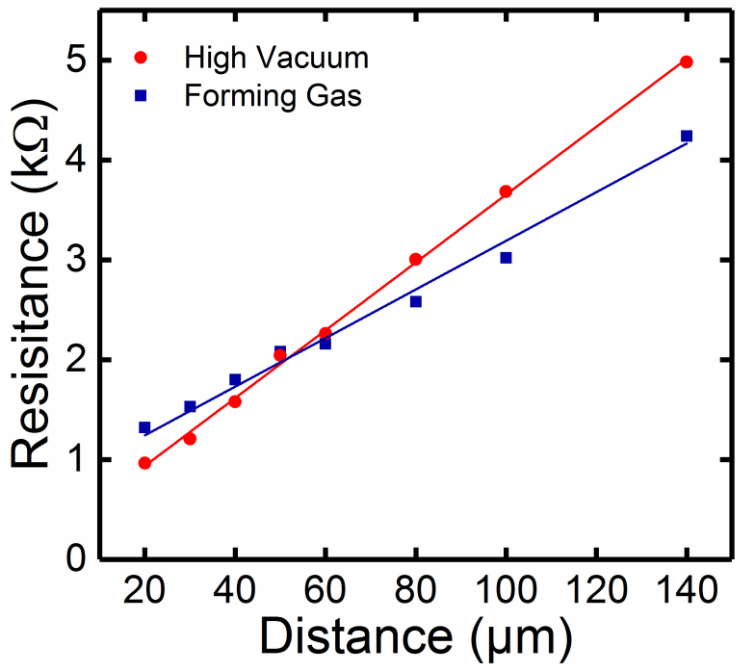


Figure 4.10: Resistance versus distance between contact pads in TLM structure for post metallisation annealing in high vacuum and forming gas ambient.

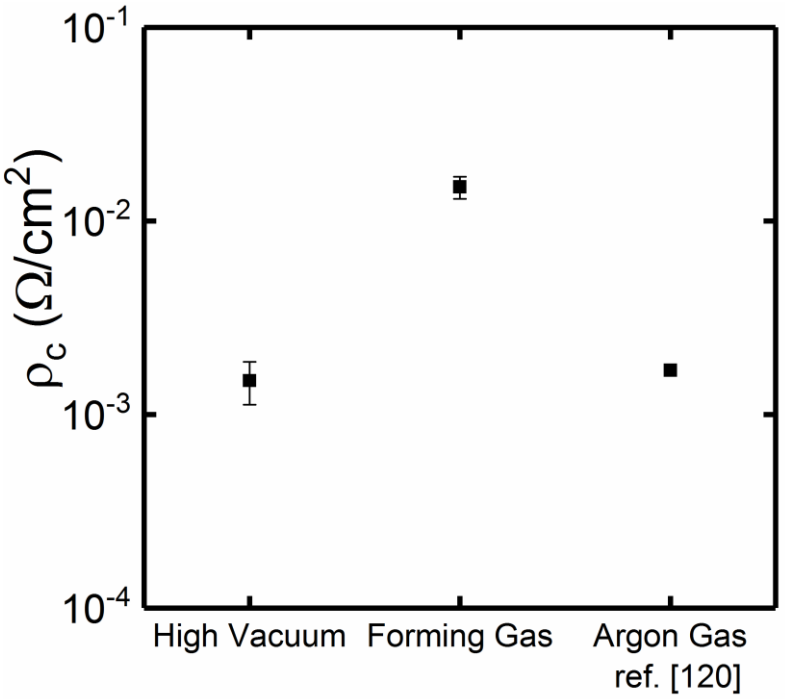


Figure 4.11: Comparison of specific contact resistivity for different process variations with Argon gas.

4.3.4 Electrical characterisation for p-type MOS capacitor

There are several types of defect related to the gate oxide. Sze and Ng [12] suggested that fixed charge (Q_f), oxide trapped charge (Q_{ot}), mobile charge (Q_m) and interface traps charge (Q_{it}) are the main causes of degraded oxide quality. These traps are attributed to the process of oxide formation including oxide growth and deposition and the type of oxide involved. Details of these traps have been discussed in section 3.2.2. Many researchers [46, 122] have reported that the poor mobility of 4H-SiC MOSFETs is due to high concentrations of interface traps (Q_{it}). These traps are located at the oxide/4H-SiC interface and are measured in terms of their density (D_{it}). Values of D_{it} above 10^{12} cm^{-2}.eV^{-1} are considered to be high and will severely affect the performance of MOS devices [7].

To determine values of D_{it}, the electrical characterisation of MOS capacitors was performed. The high–low technique was used where a frequency at 1 MHz for high and quasi-static C-V for low were applied [80, 84]. Details of this measurement have been discussed in section 3.3.3. These measurements were then corrected for series resistance as discussed in section 3.3.1.

Figure 4.12 shows the density of interface traps between 0.2–0.6 eV from the valence band edge of the 4H-SiC band gap for p-type MOS capacitor samples after high temperature

oxidation. Both samples were oxidised in an O_2 rich ambient at 1150 °C for 180 min in the furnace, resulting in SiO_2 28 nm thick using the 1150 °C oxidation technique as outlined in section 4.2.2. However, before forming a gate oxide, one of the samples experienced surface preparation and the other did not. The surface preparation process was performed by growing SiO_2 at 1150 °C for 60 min in the furnace before being completely etched using BOE for 30 s. This additional process is presumed to fully treat the surface with a new pristine layer of 4H-SiC [123]. However, based on the D_{it} distribution results shown in Figure 4.12, both devices demonstrate almost similar interface trap spectra near to the valence band edge and also across the energy level. Values of D_{it} around 2×10^{13} $cm^{-2}.eV^{-1}$ were found for both devices at 0.2 eV near to the valence band edge regardless of whether or not they had undergone surface preparation. This could suggest that the additional process using sacrificial oxide did not effectively contribute to reducing the value of D_{it}.

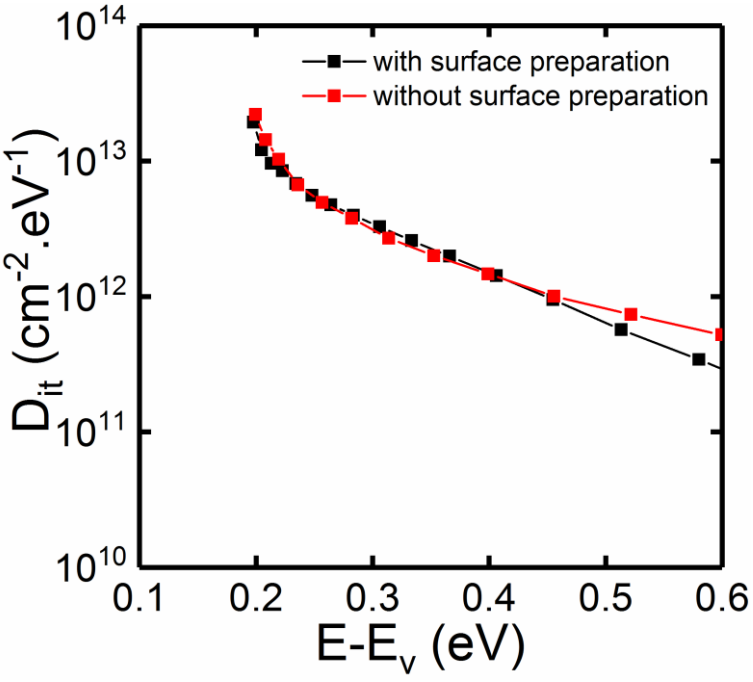


Figure 4.12: Distribution of D_{it} near the valence band edge for fabricated p-type MOS capacitor with gate oxide growth at 1150 °C for 180 min with and without surface preparation using high–low method.

For the low thermal budget device, the gate oxide was formed at a low temperature with rapid oxidation in O_2 ambient using RTP. Oxidation temperatures in a range from 600 to 800 °C in a rapid growth timeframe of 3–30 min were employed. Then a layer of Al_2O_3 40 nm thick was deposited by ALD to completely form the gate oxide. Details of the low thermal budget technique have been discussed in 4.2.1.

In order to avoid any high temperature exposure to the gate oxide after oxide growth, metal contact annealing, which required a high temperature, was performed before oxide growth. To protect the annealed metal contacts from being oxidised, 100 nm of Si_3N_4 was deposited by PECVD. This "gate last" process step allows the grown oxide to remain unharmed by the high temperature so as to keep the C defects formation as low as possible [33, 114]. To corroborate the negative impact of high temperature exposure after oxidation, MOS capacitors were fabricated with gate oxide grown before and after metallisation and PMA.

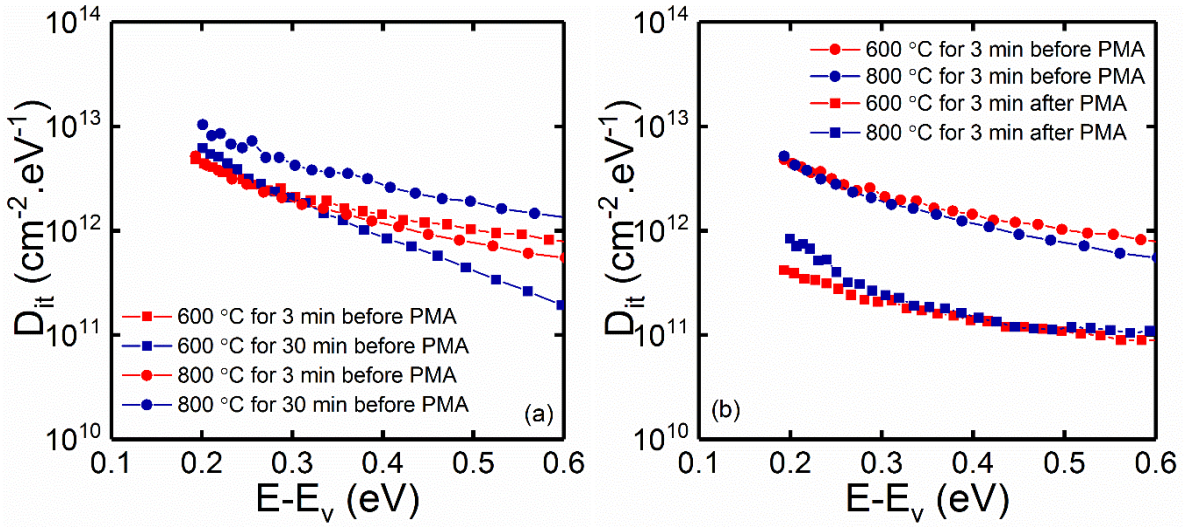


Figure 4.13: Distribution of D_{it} near the valence band edge at room temperature extracted by high-low method for the fabricated p-type MOS capacitor with gate oxide formed (a) before and (b) after post metallisation annealing using the low thermal budget method.

The results in Figure 4.13 show the distribution of D_{it} over a range of energy levels from 0.2–0.6 eV above the valence band edge within the 4H-SiC band gap. These gate oxides were grown using the low thermal budget technique. Figure 4.13 (a) demonstrates D_{it} values of gate oxide formed at 800 °C before PMA decreasing from 1.0×10^{13} $cm^{-2}.eV^{-1}$ to 5.2×10^{12} $cm^{-2}.eV^{-1}$ near to the valence band edges as the oxidation time is reduced from 30 min to 3 min. A similar trend can also be observed for the growth temperature of 600 °C, where values of D_{it} near to the valence band edges decline from 6.2×10^{12} $cm^{-2}.eV^{-1}$ to 4.8×10^{12} $cm^{-2}.eV^{-1}$ for 30 min and 3 min respectively. As the energy level increases up to 0.6 eV away from the valence band edge, the distribution of D_{it} drops gradually. Overall, these D_{it} values show a slight reduction compared to devices fabricated using the 1150 °C oxidation technique as shown in Figure 4.12. This reduction suggests that more C defects which is believed to be the source of D_{it} was generated with increasing oxidation temperature and time.

Nevertheless, even though the gate oxides were grown at low temperature for a short time, which is believed to lead to reduced D_{it} [33], the devices still experienced a high temperature process at 1000 °C for 3 min during PMA as a final fabrication step. Figure 4.13 (b) depicts the distribution of D_{it} values for devices having gate oxide grown before and after PMA using the low thermal budget technique. Similar oxidation process parameters were applied (600 and 800 °C for 3 min) in order to give a direct comparison of the effect of high temperature. The device with gate oxide growth at 600 °C for 3 min exhibited the lowest D_{it} value of 4.2×10^{11} $cm^{-2}.eV^{-1}$ at the 0.2 eV energy level above the valence band edge. In addition, a D_{it} value of 8.4×10^{11} $cm^{-2}.eV^{-1}$ was found at 0.2 eV near to the valence band edge for the device fabricated with gate oxide growth at 800 °C for 3 min. Both devices demonstrate a similar distribution of interface traps across the energy range up to 0.6 eV above the valence band edge. This represent a reduction in D_{it} by one order of magnitude compared to gate oxide formed before the PMA process with an identical oxidation temperature and time. This implies that the PMA step which involves a high temperature process has generated more C defects resulting in higher values of D_{it} even though the gate oxides were grown using the low thermal budget technique.

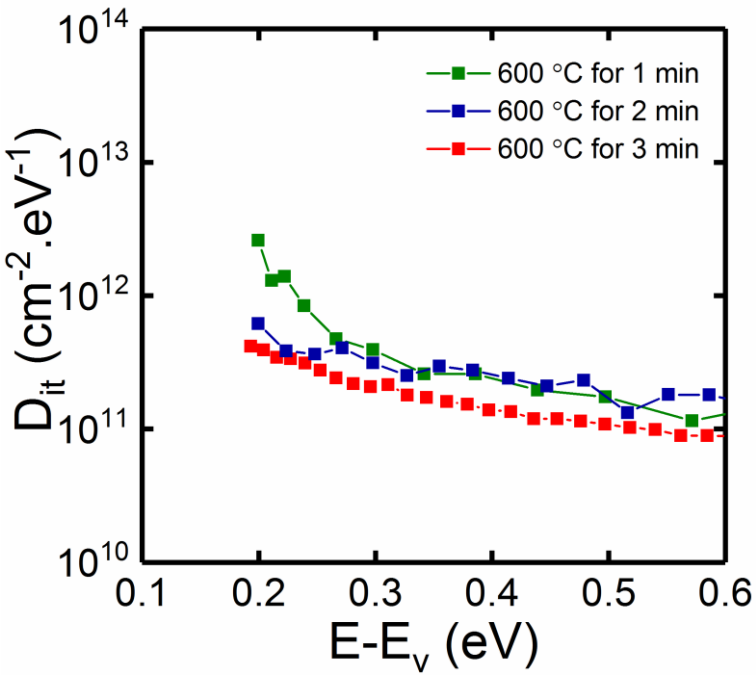


Figure 4.14: Distribution of D_{it} near the valence band edge for the fabricated p-type MOS capacitor at 600 °C for 1–3 min.

In order to further reduce the values of D_{it}, which correlates with oxide growth temperature and time, p-type MOS capacitors were then fabricated with even shorter growth timeframes of 1–3 min at the similar temperature of 600 °C. The gate oxides were formed after the metal

formation and PMA processes. Figure 4.14 shows an increase in D_{it} distribution across the energy range as the oxide growth timeframe decreases from 3 min to 1 min. An obvious difference could be seen at the energy level of 0.2 eV near to the valence band edge, where a gate oxide with a growth timeframe of 1 min gives a D_{it} value as high as 2.6×10^{12} $cm^{-2}.eV^{-1}$. A drop in D_{it} to 6.2×10^{11} $cm^{-2}.eV^{-1}$ was obtained with the oxide growth for 2 min at 600 °C. However, both D_{it} values were still higher than that for the gate oxide grown at 600 °C for 3 min with 4.8×10^{11} $cm^{-2}.eV^{-1}$ above the valence band edge. This consistently lowest D_{it} value for oxide growth at 600 °C for 3 min suggests that these oxidation parameters will reliably reduce the value of D_{it}.

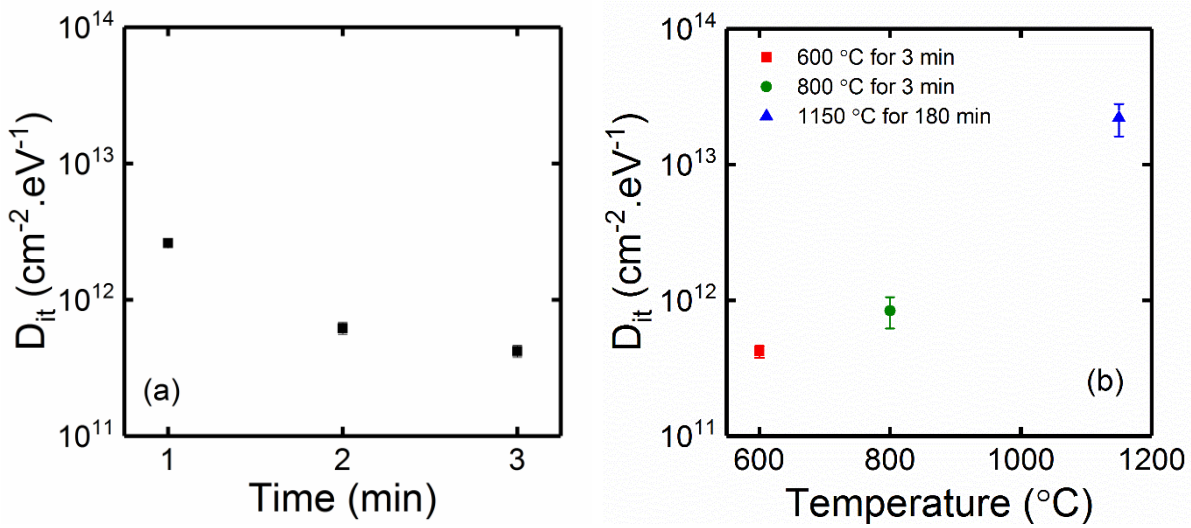


Figure 4.15: Correlation between D_{it} at energy level of 0.2 eV above the valence band edge with different growth (a) time (SiO_2 grown at 600 °C) and (b) temperature for fabricated p-type MOS capacitor using the low thermal budget technique. Additional D_{it} for gate oxide with SiO_2 grown at 1150 °C for 180 min also plotted for comparison.

Correlations between oxide growth temperature and time against interface trap density for low thermal budget devices can be clearly seen as shown in Figure 4.15. This implies that oxide grown at 600 °C for 3 min generated the lowest value of D_{it}, and hence these are the best parameters to grow the oxide using the low thermal budget technique. By using ARXPS, the thickness of the ultrathin SiO_2 layer could be estimated on those devices. Physical thicknesses of approximately 0.71, 0.63 nm and 0.58 nm were found for gate oxide grown at 600 °C for 3, 2 and 1 min respectively. Figure 4.16 depicts the correlation between D_{it} values at the 0.2 eV energy level near the valence band edge against the estimated thickness of the SiO_2 layer using ARXPS. Each point of the D_{it} value is the average from 5 different devices. Considering the trend of D_{it} distribution against estimated growth oxide thickness, the results could suggest that

the ultrathin SiO_2 layers with gate oxide grown for less than 3 min were not completely grown as well as those grown for a width of 3 min. Muller *et al*. [79] and Tang *et al*. [124] reported that, to form a complete layer state of SiO_2, at least 4 Si atoms across is required which corresponds to around 0.7 nm in physical thickness. This modelling study supports the present finding, which demonstrates that SiO_2 0.71 nm thick is the thinnest complete and useable SiO_2 layer, which thereby generated the lowest value of D_{it}.

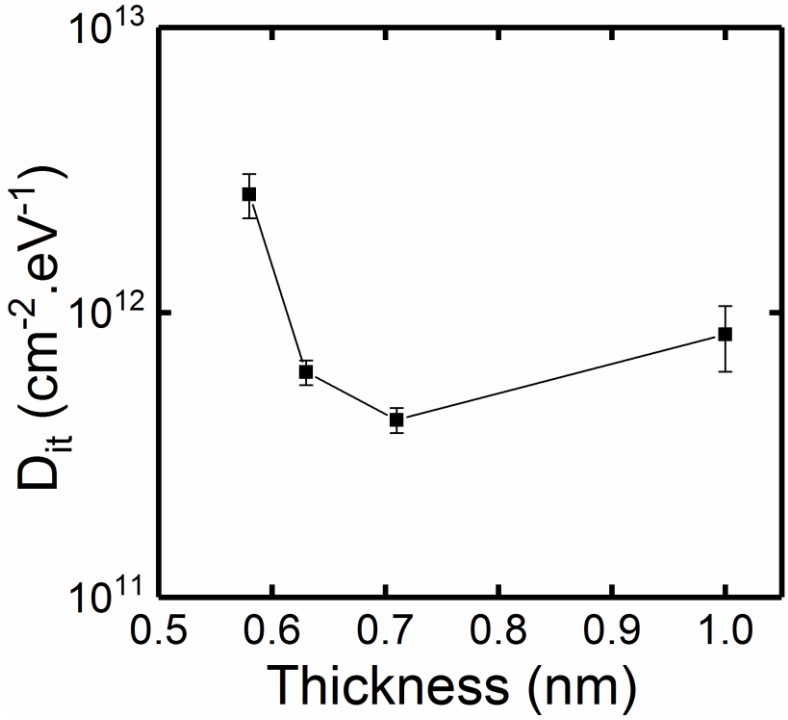


Figure 4.16: D_{it} value at energy level of 0.2 eV above the valence band edge as a function of growth thickness estimated using ARXPS for the fabricated p-type MOS capacitor using the low thermal budget technique.

Figure 4.17 shows a comparison of results for D_{it} extraction methods from the high–low and Terman techniques. Details of these extraction techniques have been discussed in section 3.3.3. By using the Terman method, the D_{it} distribution of both devices fabricated at 600 and 800 °C for 3 min were moderately increased by 1.0×10^{11} $cm^{-2}.eV^{-1}$ at an energy level of 0.2 eV above the valence band edge which is relatively small and in fact negligible. This could suggest that the D_{it} extraction approach described in this research is acceptable and comparable. Table 4.3 shows the extracted parameters for all fabricated p-type MOS capacitors using the low thermal budget technique as well as the 1150 °C oxidation technique.

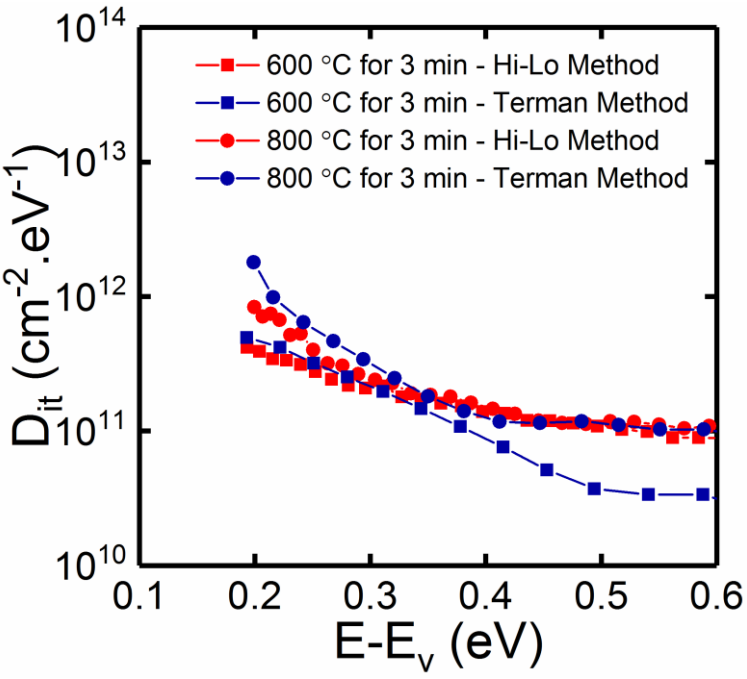


Figure 4.17: Comparison of high-low and Terman method to extract D_{it} for fabricated p-type MOS capacitor with gate oxide growth at 600 and 800 °C for 3 min.

Gate Oxide	**PMA**	**SiO_2 thickness (nm)**	**D_{it} ($cm^{-2}.eV^{-1}$)**
1150 °C for 180 min – No SP	Before	28.0	2.2×10^{13}
1150 °C for 180 min – with SP	Before	28.0	1.9×10^{13}
600 °C for 3 min	Before	0.70	4.8×10^{12}
600 °C for 30 min	Before	1.10	6.2×10^{12}
800 °C for 3 min	Before	1.10	5.2×10^{12}
800 °C for 30 min	Before	2.30	1.0×10^{13}
600 °C for 3 min (1st run)	After	0.70	4.2×10^{11}
800 °C for 3 min	After	1.00	8.4×10^{11}
600 °C for 3 min (2nd run)	After	0.71	4.8×10^{11}
600 °C for 2 min	After	0.63	6.2×10^{11}
600 °C for 1 min	After	0.58	2.6×10^{12}

Table 4.3: Extracted parameters for p-type MOS capacitor

4.3.5 Electrical characterisation of the n-type MOS capacitor

The fabrication of the n-type MOS capacitor involves a low thermal budget as well as the 1150 °C oxidation technique similar to that for the p-type MOS capacitor as outlined in section 4.2. An additional nitridation treatment step was performed on one of the samples fabricated using the 1150 °C oxidation method. The post oxidation annealing in N_2O was assumed to passivate the interface traps and remove any C related defects thus enhancing the interface state quality [42, 125]. Details of the fabrication process have been discussed in section 4.2.3.

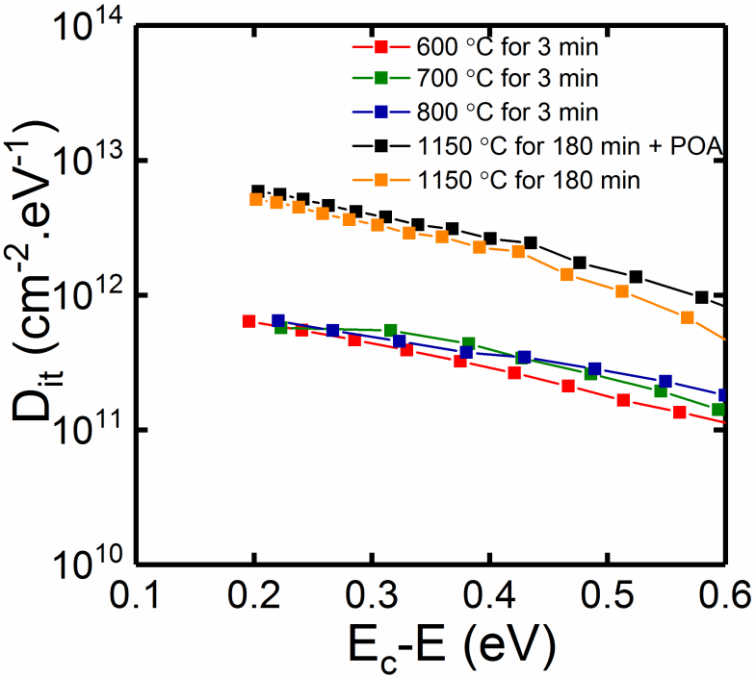


Figure 4.18: Distribution of D_{it} near the conduction band edge for the fabricated n-type MOS capacitor with different gate oxide growth conditions using the high-low method.

Figure 4.18 shows the distribution of interface traps as a function of energy level near to the conduction band edge for the fabricated n-type MOS capacitor with different gate oxide growth conditions. The extracted values of D_{it} over the range between 0.2–0.6 eV were determined from the C-V characteristics using the high-low method. This data indicates a huge difference between the D_{it} spectra for the low thermal budget and 1150 °C oxidation techniques. For 1150 °C oxidation devices, D_{it} values of approximately 5.0×10^{12} $cm^{-2}.eV^{-1}$ were found at 0.2 eV near to the conduction band edge irrespective of the use of POA in N_2O. This suggests that the additional post oxidation annealing process does not contribute to reducing the value of D_{it}. A higher annealing temperature (> 1250 °C) is needed to effectively reduce the D_{it} using this method [44]. In contrast, devices that have ultrathin SiO_2 layers exhibit lower concentrations of D_{it} of about 6.0×10^{11} $cm^{-2}.eV^{-1}$ at 0.2 eV near to the conduction band

edge regardless of oxide growth temperature. However, as the energy level increases, a slight drop was observed for the gate oxide grown at 600 °C for 3 min. This could suggest that the concentration of interface traps has been reduced in the deeper level of the band gap. Overall, a reduction in D_{it} by 1 order of magnitude was achieved for low thermal budget devices over the energy range of 0.2–0.6 eV below the conduction band edge compared to the 1150 °C oxidation technique devices.

Then, n-type MOS capacitors were fabricated with different oxide growth timeframes at 600 °C to further reduce the value of D_{it}. Figure 4.19 demonstrates the D_{it} distribution for n-type MOS capacitors fabricated for 1–5 min at 600 °C versus energy level close to the conduction band edge. No significant differences are observed in D_{it} with gate oxide grown for 2–5 min at 600 °C. However, devices that experienced oxide growth for 1 min at 600 °C exhibited an apparent rise in values of D_{it} over the range of energy levels. A D_{it} value of 1.6×10^{12} $cm^{-2}.eV^{-1}$ at 0.2 eV was found for this gate oxide compared with the others which displayed values of around 6.0×10^{11} $cm^{-2}.eV^{-1}$. This different value of D_{it} could be ascribed to the incomplete formation of the SiO_2 layer, which requires at least 4 Si bonds to correspond to a layer thickness 0.7 nm [79, 124]. This result is in agreement with those for the p-type MOS capacitor as discussed in section 4.3.4.

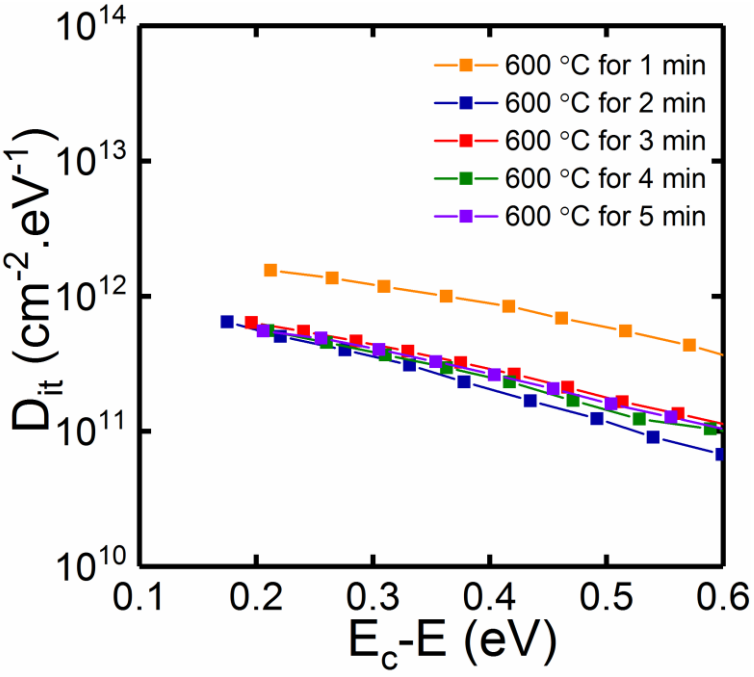


Figure 4.19: Distribution of D_{it} near the conduction band edge for the fabricated n-type MOS capacitor with gate oxide growth at 600 °C for 1-5 min using the high-low method.

4.3.6 High temperature measurements of p-type and n-type MOS capacitors

4H-SiC is a wide band gap semiconductor which is able to operate in high temperature [24] and harsh environments [6]. Many applications require 4H-SiC MOS devices to operate at high temperatures such as in the military and outer space sectors. Thus, MOS devices must be very reliable and stable at high temperatures in order to ensure that performance is not compromised under such hostile conditions.

In this section, p-type and n-type MOS capacitors with gate oxides fabricated using a low thermal budget method and 1150 °C oxidation technique are examined in order to observe their behaviour over a wide range of temperatures. Gate oxides were grown at 600 °C and 800 °C for 3 min using low thermal budget method followed by Al_2O_3 deposition. For comparison, gate oxides which were grown in the furnace at 1150 °C for 180 min are also shown. Measurements at room temperature show that the low temperature gate oxides exhibit lower values of D_{it} compared to 1150 °C devices, as described in 4.3.4. Figure 4.20 shows the density of oxide capacitance (C_{ox}) for the fabricated (a) p-type and (b) n-type MOS capacitors extracted from their C-V characteristics at 1 MHz in the accumulation region as a function of temperature between 25 °C and 300 °C. Each point of the C_{ox} value is the average from 5 different devices. C_{ox} values of approximately 126 nf/cm^2 which correspond to an EOT of 28 nm were obtained over wide range of elevated temperatures. The results indicate that all of the fabricated devices with both p-type and n-type MOS capacitors exhibit excellent oxide stability during high temperature conditions.

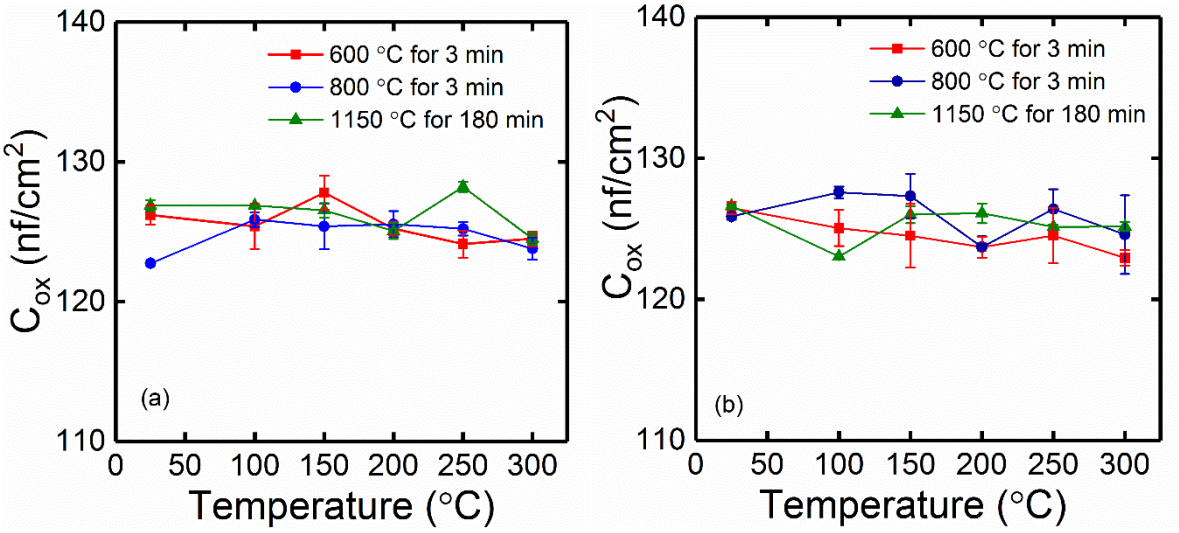


Figure 4.20: Density of oxide capacitance measured at 1 MHz for (a) p-type and (b) n-type MOS capacitor as a function of temperature.

Figure 4.21 shows the C-V characteristics for the forward sweep n-type MOS capacitors with gate oxide growth at 600 °C for 3 min + 40 nm of Al_2O_3 and 1150 °C for 180 min against elevated temperature. The C-V curve for the MOSFET with gate oxide grown at 600 °C for 3 min shifts towards positive as the measured temperature increases up to 100 °C before changing its direction to a negative shift with further increases in temperature up to 300 °C. Overall, the C-V curves for both devices shift towards zero gate voltage with increasing temperature, and the device with gate oxide grown at 600 °C for 3 min demonstrates significant changes over the measured temperature range compared with the 1150 °C device. These changes were observed as a flatband voltage (V_{fb}) change in elevated temperatures and will discuss in detail later.

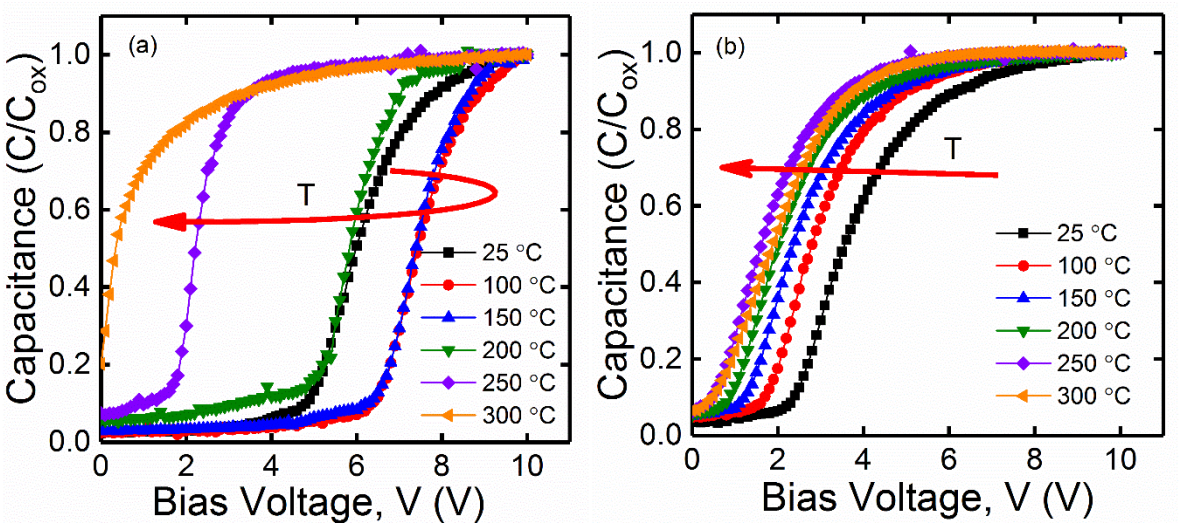


Figure 4.21: C-V characteristics for forward sweep of fabricated n-type MOS capacitor with oxide growth at (a) 600 °C for 3 min and (b) 1150 °C for 180 min plotted against elevated measured temperature.

Data from Figure 4.22 shows the V_{fb} during the forward and reverse sweeps for gate oxides grown at 600 °C and 800 °C for 3 min as well as at 1150 °C for 180 min versus elevated temperature measured up to 300 °C. Each point of the V_{fb} value is the average from 5 different devices. The V_{fb} at each temperature was extracted from C-V characteristics during the accumulation region as discussed in section 3.3.1. The V_{fb} for the forward and reverse sweeps of the p-type MOS with gate oxide grown at 1150 °C was stable over the measured temperature range. Both sweeps show a V_{fb} of approximately - 10 V at room temperature which changes by ± 2 V up to the measured temperature at 300 °C. In contrast, the V_{fb} of gate oxide from the low thermal budget process were significantly increased from - 14 V and - 9 V at room temperature to - 2 V at 300 °C for devices with oxide grown at 600 °C and 800 °C respectively.

A similar trend could be observed in V_{fb} for n-type MOS devices in both the forward and reverse sweeps. The devices with gate oxide grown at high temperature demonstrate a slight reduction towards 0 V from 4 V at 25 °C to about 2 V at the high temperature of 300 °C. However, a substantial decrease by 5 V was observed in low thermal budget devices over the measured temperature range up to 300 °C.

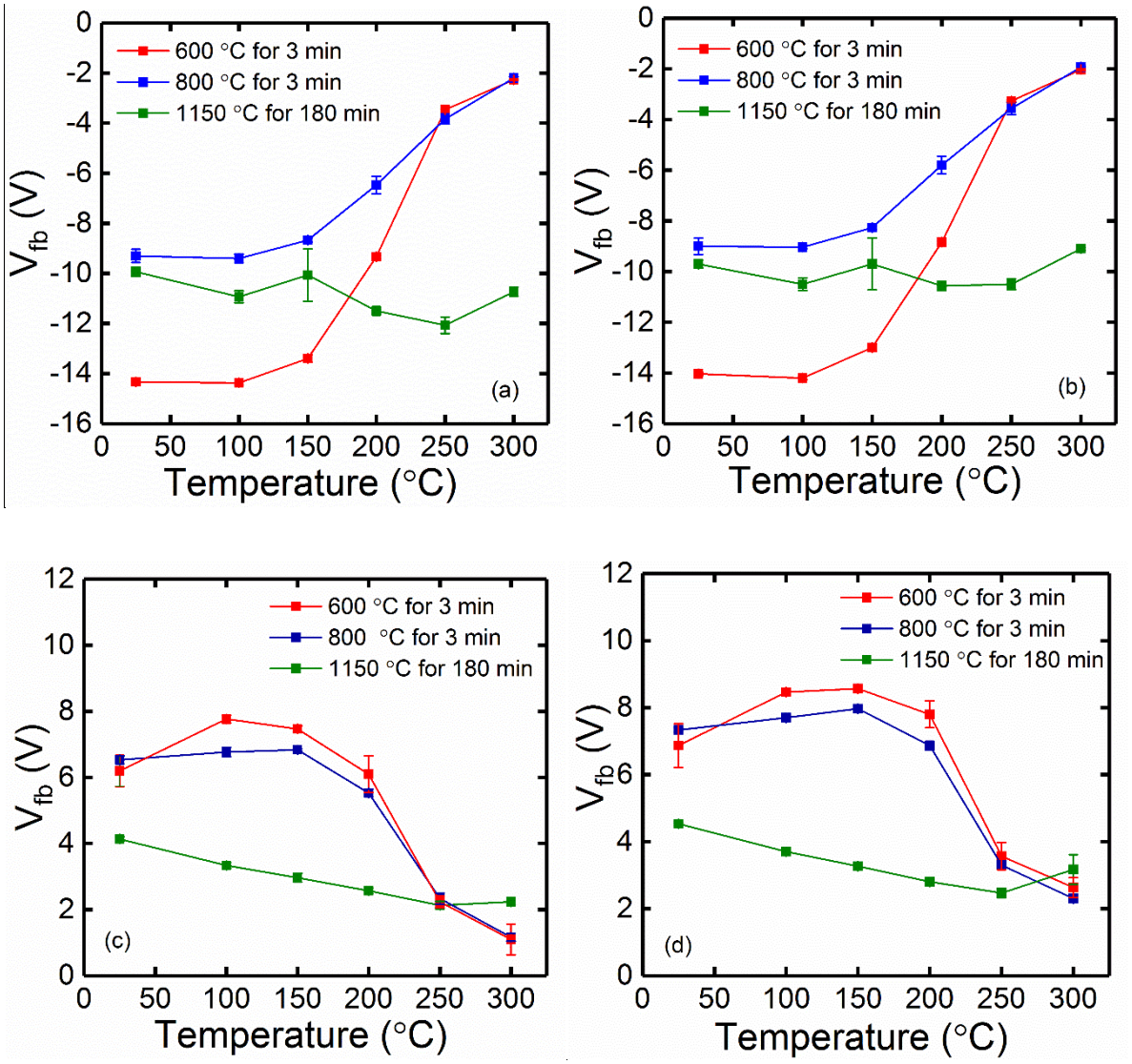


Figure 4.22: V_{fb} measured at 1 MHz for (a) forward sweep and (b) reverse sweep for p-type and (c) forward and (d) reverse sweep for n-type MOS capacitor versus temperature

These changes in V_{fb} over the temperature range can be attributed to the charges present in the bulk oxide including fixed charge, Q_f, oxide trap charge, Q_{ot} and mobile charge, Q_m, as discussed in section 3.2.2.

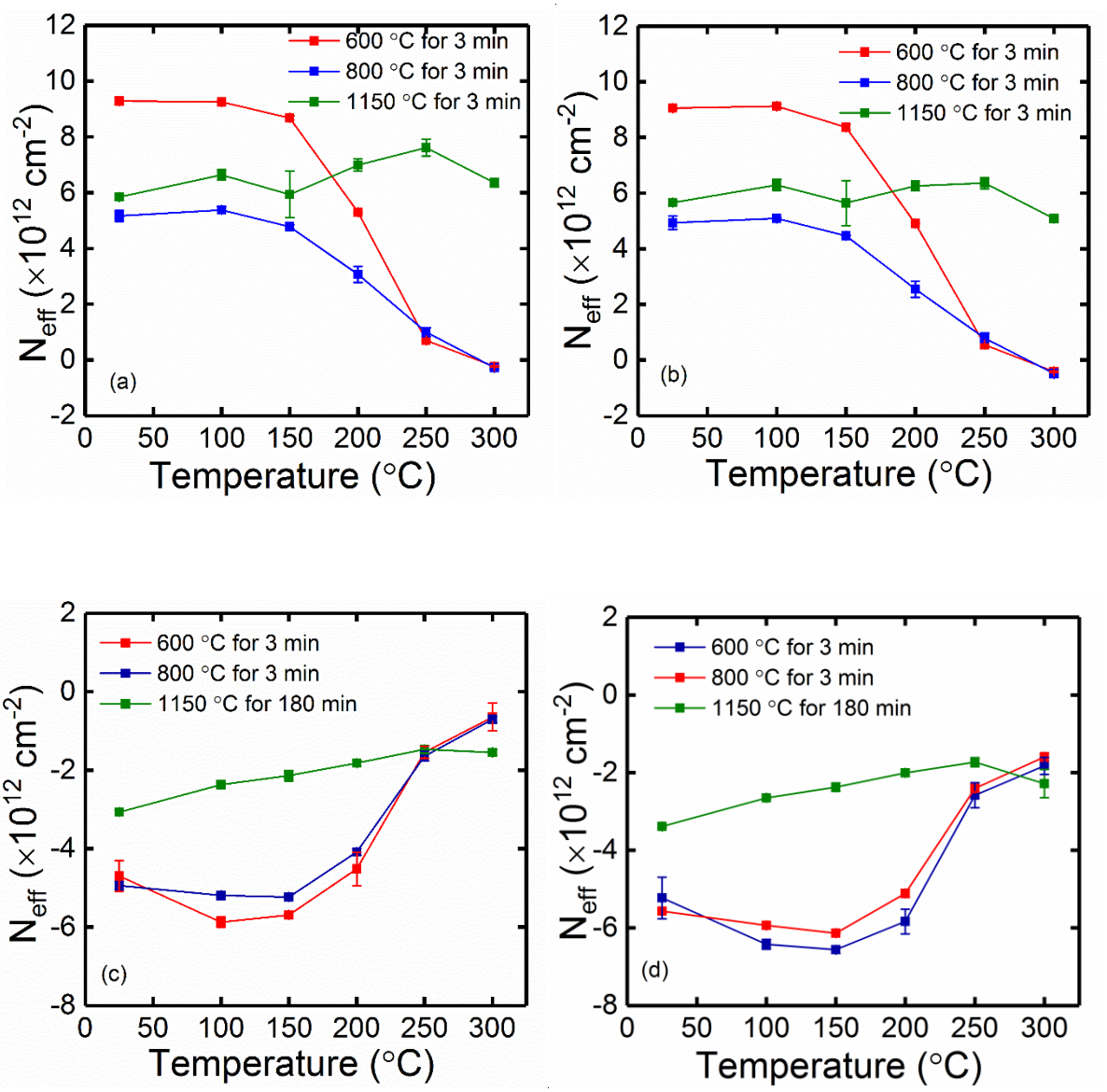


Figure 4.23: Effective oxide charge N_{eff}, measured at 1 MHz for (a) forward sweep and (b) reverse sweep for p-type and (c) forward and (d) reverse sweep for n-type MOS capacitors versus temperature

Figure 4.23 shows the N_{eff} of the fabricated MOS capacitors extracted from C–V characteristics measured at 1 MHz using equation 3.29 as a function of temperature. Each point of the N_{eff} value is the average from 5 different devices and the gate metal work function, ϕ_{Al} = 4.1 eV. These results indicate that the values of N_{eff} in devices with an ultrathin layer of SiO_2 decreased significantly with increasing temperature from about 9.0×10^{12} cm^{-2} for those grown at 600 °C and 5.0×10^{12} cm^{-2} for those at 800 °C to 6.0×10^{11} cm^{-2} with increasing temperature up to 250 °C before changing polarity to -3.0×10^{11} cm^{-2} at 300 °C for both sweeps of the p-type MOS capacitors. In contrast, devices with gate oxide grown at 1150 °C displayed more or less similar values of N_{eff} at around 6.0×10^{12} cm^{-2} at various elevated

measured temperatures. Similar behaviour also could be noticed in n-type MOS capacitors for low thermal budget and standard high temperature gate oxide devices. These substantial changes N_{eff} for low thermal budget devices may be due to the nature of bulk Al_2O_3, which can have 5 stable charge states of O vacancy [126].

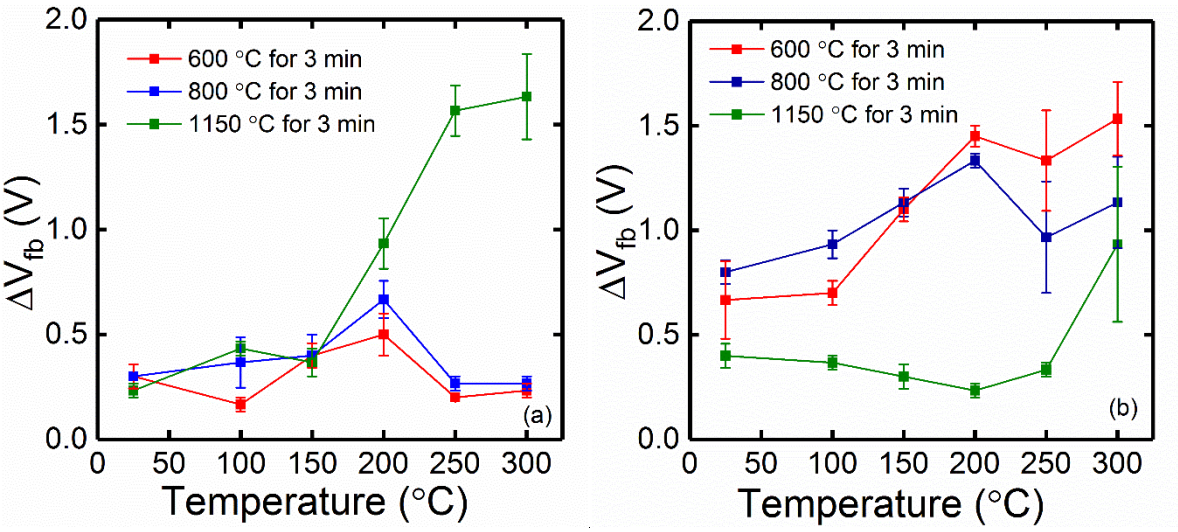


Figure 4.24: Change in flatband voltage, ΔVfb extracted at 1 MHz for fabricated (a) p-type and (b) n-type MOS capacitors as a function of temperature.

Figure 4.24 shows the hysteresis of flatband voltage (ΔV_{fb}) calculated from the differences in V_{fb} between the forward and reverse sweeps for (a) p-type and (b) n-type MOS capacitors as a function of elevated temperature. Each point of the ΔV_{fb} value is the average from 5 different devices. For p-type MOS capacitors having an ultrathin SiO_2 layer of gate oxide, ΔV_{fb} was relatively stable with values less than 0.7 V with increasing temperature. Conversely, ΔV_{fb} increased steadily by 1 V from 25 °C to 300 °C for ultrathin gate oxide n-type devices, This variation in trends can be explained by the effect of electron trapping and de-trapping, which are known to happen in the Al_2O_3 [126]. For gate oxide grown at 1150 °C, the values of ΔV_{fb} were stable at less than 0.5 V from 25 °C before significantly surging at 200 °C and 300 °C for p-type and n-type devices respectively. This suggests that the electron trapping and de-trapping effect is also present in thermally grown SiO_2 gate oxide but started to rise beyond a certain temperature.

Figure 4.25 shows the density of interface traps, D_{it} at the 0.2 eV energy level near to (a) the valence and (b) conduction band edges as a function of elevated temperature. Each point of the D_{it} value is the average from 5 different devices. The high–low method was used to extract the values of D_{it} of the fabricated devices at each measured temperature. All p-type and

n-type MOS devices demonstrated a slight reduction in D_{it} with increasing temperature up to 300 °C. This suggests that the interface trap charges are electrically excited at elevated temperature. In addition, as the temperature increases, the bandgap shrinks and becomes narrow so as to reduce the concentration of interface traps at the band edges [127]. The reduction of bandgap with temperature is shown in Figure 3.3. This effect also occurs in Si-SiO_2 systems as temperature increases [128].

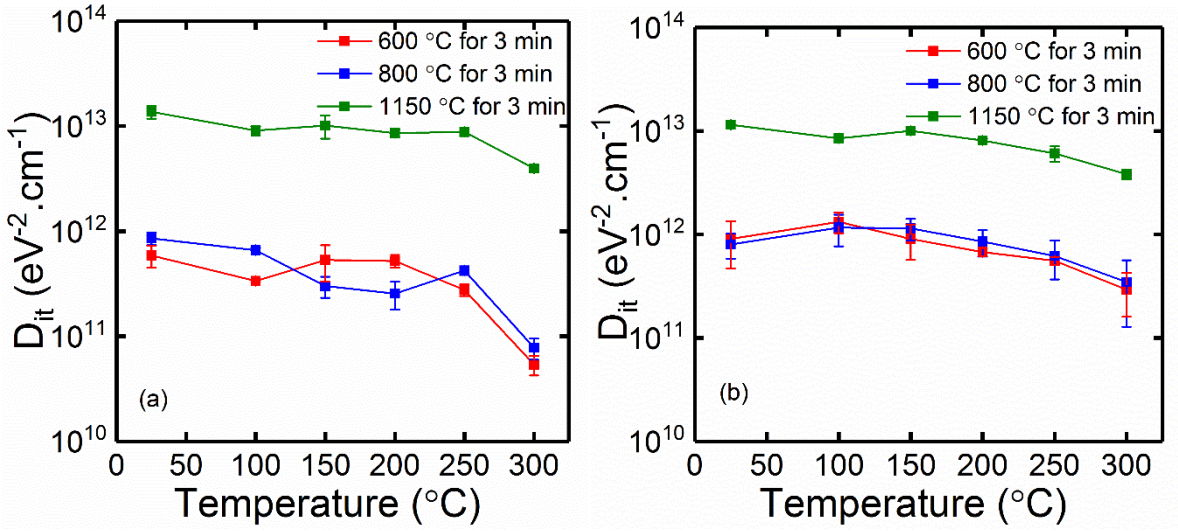


Figure 4.25: Values of D_{it} at the 0.2 eV energy level near to the (a) valence and (b) conduction band edge versus temperature.

4.3.7 Current conduction mechanism

I-V characterisation was performed to determine the current conduction mechanism of the fabricated gate oxide of the devices. Figure 4.26 shows the leakage current density under positive gate biases for gate oxide fabricated at 600 °C for 1–3 min using low the thermal budget technique. The gate oxide which consists of an ultrathin SiO_2 layer grown at 600 °C for 3 min was able to withstand an oxide field of 6.5 MV/cm with a leakage current density of approximately 1×10^{-8} A/cm^2. However, the breakdown oxide field was reduced to 2 MV/cm at a leakage current density of 1×10^{-8} A/cm^2 as the growth timeframe decreased to 2 and 1 min. For devices with a 2 min timeframe, multiple stages happened whereas soft and hard oxide breakdown occurred at 2 MV/cm and 6.4 MV/cm respectively. In addition, the ultrathin SiO_2 grown at 4 and 5 min could withstand oxide electric field up to 8.5 and 10 MV/cm, but the electron tunnelling started to occur at lower field suggesting large concentration of trap charges with these gate oxides. This could suggest that a sufficient growth timeframe of 3 min at 600 °C is required to form a complete ultrathin SiO_2 layer 0.7 nm thick which could

withstand higher oxide fields [79, 124]. The capability to operate in high oxide fields is important, since the actual operating oxide field for 4H-SiC MOS devices is 3 MV/cm [50, 129].

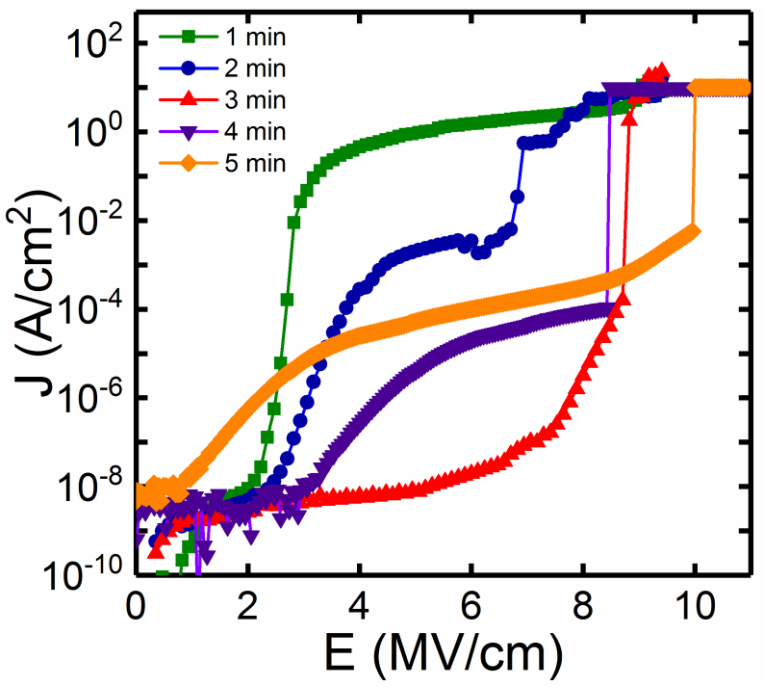


Figure 4.26: Current density as a function of the oxide field of fabricated n-type MOS capacitors with SiO_2 grown at 600 °C for different duration using the low thermal budget technique

In order to further investigate the leakage current mechanism at high field for fabricated n-type MOS capacitors with oxide grown at 600 °C for 3 min, the Fowler-Nordheim (F-N), Poole-Frenkel (P-F) and Trap Assisted Tunnelling (TAT) emission were plotted. Those plots were obtained from I-V characteristics and the analysis was based on linear fitting between 6.8 and 8.3 MV/cm. The F-N tunnelling current density can be expressed as equation 4.1 [130-132]:

$$J_{FN} = AE^2 \exp\frac{-B}{E} \tag{4.1}$$

where

$$A = \frac{q^3 m}{8\pi\hbar m_{ox}\phi_B} \tag{4.2}$$

$$B = \frac{8\pi\sqrt{2m_{ox}}\phi_B}{3\hbar q} \tag{4.3}$$

where q = electron charge, ħ = reduced Planck constant, m is the effective electron mass in the 4H-SiC, m_{ox} = 0.2m_o [133, 134] is the effective electron mass in the oxide and ϕ_B is the effective barrier height. Barrier height (ϕ_B) which controls the current conduction in the F-N mechanism, is defined between the conduction band edge of 4H-SiC and the oxide [135]. Figure 4.27 shows an excellent linear relationship over three magnitudes of current, suggesting that F-N electron tunnelling dominates the current conduction mechanism in high field [12, 136]. By fitting the F-N plot, ln (J/E^2) as a function of 1/E as equation 4.4, ϕ_B can be obtained.

$$\ln\left(J/E\right) = \ln(A) - B/E \tag{4.4}$$

In this study an ϕ_B of 1.35 eV was found for the gate stack. This value is in agreement with those of previous reports by Tanner *et al.* [133] and Khosa *et al.* [137], where the values of ϕ_B were 1.58 eV and 1.15 eV respectively for Al_2O_3 gate oxide extracted using F-N fitting at high field.

In addition Poole-Frenkel (P-F) and Trap Assisted Tunnelling (TAT) emissions were also investigated to further understand the current conduction mechanism. The P-F emission plot can be expressed as in equation 4.5 [12].

$$\ln\left(J/E\right) = \frac{q}{kT}\sqrt{\frac{q}{\pi\varepsilon_o\varepsilon_r}}\sqrt{E} - \frac{q\phi_t}{kT} + \ln(q\mu N_C) \tag{4.5}$$

where N_C, μ, ϕ_t, ε_r, ε_o and k are the density of states in the conduction band, electron mobility in the oxide, trap energy level, dielectric constant of the oxide, dielectric constant of vacuum and Boltzmann's constant respectively.

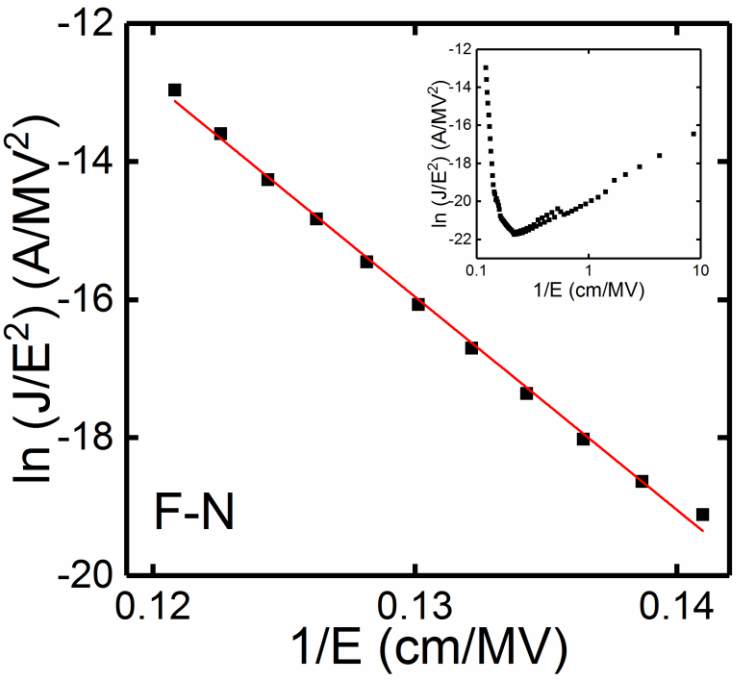


Figure 4.27: Fowler−Nordheim plot (inset: extended Fowler−Nordheim plot), for fabricated n-type MOS capacitors with oxide grown at 600 °C for 3 min using the low thermal budget technique.

Figure 4.28 (a) depicts a linear relationship in the Poole-Frenkel plot, suggesting that this mechanism may contribute to the leakage current. However, using P-F fitting, the extracted effective relative permittivity for the SiO_2/Al_2O_3 gate stack is too large where, $\varepsilon_r = 102$. This suggests that Poole-Frenkel tunnelling cannot be responsible in this gate oxide [136]. Another well-known bulk limited emission, trap assisted tunnelling was also studied. The trap assisted tunnelling plot can be show as equation 4.6:

$$\ln(JE) = \left(\frac{8\pi\sqrt{2m_{ox}}\phi^{3/2}}{3\hbar q}\right)\left(1/E\right) + \ln\left(\frac{2}{3}qC_tN_t\phi_t\right) \qquad (4.6)$$

where C_t is also called the trap energy-dependent rate constant. A good linear correlation was observed in the TAT plot shown in Figure 4.28 (b), but the extracted trap energy level, ϕ_t = 15.6 eV, which is larger than the theoretical bandgap of Al_2O_3 (E_g = 7 – 8.9 eV) and SiO_2 (E_g = 9 eV) [12]. This suggests that TAT emission does not dominate the current conduction mechanism in the gate stack.

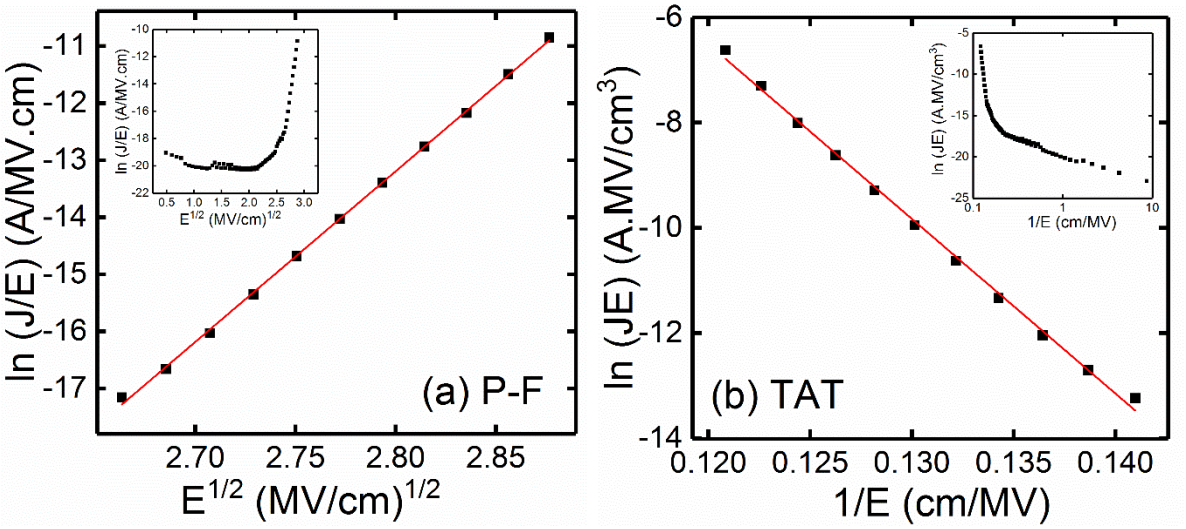


Figure 4.28: (a) Poole-Frenkel plot (inset: extended Poole-Frenkel plot), and (b) Trap-Assisted-Tunnelling plot (inset: extended Trap Assisted Tunnelling plot) for fabricated n-type MOS capacitors with oxide grown at 600 °C for 3 min using the low thermal budget technique.

4.4 Key Findings and Conclusion

4H-SiC MOS capacitors were successfully fabricated on p-type and n-type SiC epitaxy using several process steps. From the results, the hypothesis that thermally grown SiO_2 generates C_i that can eventually bind to each other and form immobile clusters $(C_i)_2$ which may contribute to higher D_{it} value is possible. Additional process steps by performing post-metallisation annealing before the oxidation process is beneficial for reducing D_{it} by one order of magnitude. The density of interface states show values as low as 4.2×10^{11} $cm^{-2}.eV^{-1}$.These are obtained from the lowest oxidation temperature at 600 °C for 3 min. Further investigation was conducted by reducing the oxidation time down to 1 min and keeping the oxidation temperature at 600 °C. The D_{it} distribution at an energy level of 0.2 eV recorded the lowest trap density for a growth time of 3 min of 4.8×10^{11} $cm^{-2}.eV^{-1}$. Then a similar trend was observed with n-type MOS capacitors where this oxidation condition generated the lowest D_{it} with a value of 6.0×10^{11} $cm^{-2}.eV^{-1}$. This D_{it} distribution result was shown to be consistent at the 3 min duration of oxidation at 600 °C with grown 0.7 nm oxide, proving that these are the best parameters to use.

All devices demonstrated a highly stable C_{ox} during measurement at high temperature. The V_{fb} shift towards 0 V with increasing temperature may be due to the presence of N_{eff} in the bulk. Variation in hysteresis was observed for the gate oxide having an ultrathin SiO_2 layer over the range of elevated temperatures. The well-known nature of Al_2O_3 have contributed to

this effect. Values of D_{it} were reduced as the temperature increased, mainly owing to electron excitation from the traps and a narrowing bandgap effect. In addition, the MOS gate stack with oxide grown at 600 °C for 3 min produced an effective barrier height, ϕ_B, of 1.35 eV and it was able to withstand electric fields of 6.5 MV/cm with a leakage current density of around 1×10^{-8} A/cm^2, thereby demonstrating that this gate oxide stack is robust.

Ultrathin layers of oxide of thicknesses 0.5 nm ~ 2 nm were successfully grown and confirmed by ARXPS. MOS devices with oxide thickness of 28 nm were also fabricated in the oxidation furnace at 1150 °C as control samples for comparison purposes. The deposition of Al_2O_3 on top of the grown oxide was effectively deposited by ALD at 200 °C with 500 cycles in order to obtain around 40 nm of Al_2O_3. An optimized Al/Ti stack with a weight ratio of 3:1 for ohmic contact to p-type epitaxial 4H-SiC ($N_A = 1 \times 10^{17}$ cm^{-3}) was also achieved. A minimum specific contact resistivity of 1.5×10^{-3} Ω.cm^2 was obtained after annealing in high vacuum at 1000 °C for 3 min.

In electrical measurements, all samples exhibited good metal oxide semiconductor (MOS) behaviour from C-V measurement. In conclusion, devices fabricated using the low thermal budget technique have demonstrated a good quality of grown oxide. Values of D_{it}, which is correlated to poor electron mobility in 4H-SiC MOSFETs, has been successfully reduced using this technique. The high concentrations of interface traps in thermally grown devices suggest that C defects are generated by high oxidation temperature.

Chapter 5

4H-SiC MOSFETs Using Ultrathin SiO_2/Al_2O_3 Gate Stack

5.1 Introduction

After developing a gate stack of Metal Oxide Semiconductor (MOS) capacitors that generated less density of interface traps (D_{it}), focus will now shift to fabricate Metal Oxide Semiconductor Field Effect Transistors (MOSFETs) using similar technique. As a wide bandgap semiconductor material, Silicon Carbide (SiC) could provide many desirable properties in MOSFET technology, offering significant advantages over Silicon (Si) MOSFETs particularly for applications in power electronics [138] and electronics for harsh environments [139]. But high-quality oxide-semiconductor interfaces have been a major challenge in the fabrication of SiC MOSFETs. By contrast, the excellent interface formed between Si and Silicon Dioxide (SiO_2) has led to the success of CMOS technology, and even in the era of high-k dielectrics an interfacial SiO_2 layer is introduced to improve the Si interface quality [126]. In SiC MOSFETs, electrically active defects close to the SiC/oxide interface have led to poor electron mobilities, typically below 10 $cm^2/V{\cdot}s$ [36, 37]. Usually a gate oxide is fabricated by the high temperature oxidation of SiC in dry oxygen (O_2) [7]. This produces a range of defects such as residual Carbon (C), dangling bonds and complex C clusters that are difficult to eradicate [33, 110]. Oxide nitridation using post oxidation annealing (POA) is commonly used to mitigate these defects, but this is only partially successful, leading to mobilities in the range of 30-40 $cm^2/V{\cdot}s$ [36, 37]. An alternative approach has been to use a deposited high-k dielectric such as Al_2O_3 to replace the thermally grown SiO_2. Hatayama *et al.*[34] claimed field effect mobilities as high as 294 $cm^2/V{\cdot}s$ in SiC MOSFETs utilising a SiO_2

interfacial layer between SiC and a deposited Al_2O_3 dielectric. They concluded that an interfacial oxide layer with a thickness above 2 nm degrades the interface and channel mobility. Lichtenwalner *et al.*[67] obtained field effect mobilities as high as 106 $cm^2/V{\cdot}s$ using a 25 nm Al_2O_3 layer formed by Atomic Layer Deposition (ALD). The interface state defect density (D_{it}) was controlled by high temperature annealing in nitric oxide (NO) prior to Al_2O_3 deposition. This had the consequence of forming an interfacial oxide of a thickness 1–2 nm. But in both of these cases [34, 67] the high peak mobility drops to less than 50% of its maximum value when the gate-source voltage (V_{GS}) is increased by 1 V, which will compromise device performance. Zheng *et al.*[64] have recently used borosilicate glass (BSG) as a gate dielectric, obtaining a peak field-effect mobility of 180 $cm^2/V{\cdot}s$ when BSG is combined with Antimony (Sb) counter-doping in the channel, but mobility again declines rapidly with increasing V_{GS}.

In this chapter, SiC MOSFETs have been fabricated having a peak field effect mobility of 125 $cm^2/V{\cdot}s$, which degrades less severely than the previously reported high mobility SiC MOSFETs mentioned above [34, 64, 67]. Therefore its impact on device performance is improved, leading to drain current enhancements of up to 120× compared with control devices fabricated using an oxidation at 1150 °C. By using gate oxidation at a low temperature of 600 ºC and for a short time of 3 min, the resulting interfacial oxide layer thickness is 0.7 nm, thereby limiting the formation of defects in the SiC. Shen and Pantelides [33] proposed that immobile C di-interstitial defects $(C_i)_2$ form in SiC as a result of thermal oxidation. Defects of this kind would go some way to explain the poor channel mobility observed in SiC MOSFETs even following post oxidation annealing (POA). Mobility will also be degraded by remote Coulombic scattering, which is a particular issue for deposited dielectrics such as Al_2O_3 [126]. By carrying out a POA of our deposited Al_2O_3 dielectric, remote Coulombic scattering is reduced. Charged defects also have a deleterious effect on the subthreshold slope (SS) [12]. Where reported [11], SS can be more than 10× larger than the ideal value of 60 mV/dec for long channel (> 100 µm) SiC MOSFETs, indicating high levels of charged defects even when peak mobility is high. We found that SS = 130 mV/dec for a 2 µm gate length SiC MOSFET, which is consistent with reduced levels of charged defects.

5.2 Experimental Details

The n-channel planar MOSFETs were fabricated on epitaxial 4H-SiC wafers supplied by Cree (3.84° off-axis, Si-face, n^+ (sub)/p^+ (10^{17} cm^{-3}, 5 µm)/p^- (5.3×10^{15} cm^{-3}, 1 µm). After standard organic, Piranha and RCA cleaning, the source and drain regions were formed by multi-energy nitrogen (N) ion implantation to form a box doping profile (4.7×10^{19} cm^{-3}, 100 nm). The

implantation was performed at room temperature with the ion beam perpendicular to the surface and through a 30 nm thick Aluminium (Al) layer deposited on the samples. After the removal of the implantation mask and Al layer, a graphite capping layer [140] was used to protect the samples during activation annealing at 1700 ºC for 10 min. To minimize any possible SiC surface oxidation, the protective layer was then removed by cleaning in a Tegal PLASMOD 100 W Tabletop Plasma Reactor at room temperature for 90 min, followed by another RCA cleaning. After that, the source and drain contacts were formed by e-beam evaporation of 5 nm thick Ti and 90 nm thick Ni, followed by annealing in vacuum at 1000 ºC for 3 min as depicted in Figure 5.1(a). To protect the metal from being oxidised, 100 nm of Si_3N_4 was deposited by Plasma Enhanced Chemical Vapour Deposition (PECVD) as shown in Figure 5.1(b) [116]. The deposited Si_3N_4 was removed by BHF in the channel region, and immediately a thin SiO_2 layer was grown at 600 ºC for 3 min by Rapid Thermal Processing (RTP) in a dry O_2 ambient as depicted in Figure 5.1(c). This was immediately followed by the growth of around 40 nm of Al_2O_3 by ALD to achieve an effective oxide thickness (EOT) of 29 nm for the gate stack as shown in Figure 5.1(d). Adduct-grade trimethylaluminium (TMA) and H_2O were used as precursors and transported to the reaction chamber by vapour draw with N_2 carrier gas. Deposition was performed at 200 ºC, at a chamber pressure of 600 mTorr, with pulse/purge lengths of 0.1/4 s and 0.1/6 s for TMA and H_2O respectively. Then, Al_2O_3 and Si_3N_4 layers were etched to open source and drain contacts as shown in Figure 5.1(e). The devices were completed with the deposition of 150 nm of Al to form the gate contacts and post deposition annealing was performed in nitrogen ambient at 300 ºC for 60 min as depicted in Figure 5.1(f).

Alongside fabrication of the "thin-SiO_2" devices described above, "thick-SiO_2" control MOSFETs were fabricated having a conventional high temperature oxidation. The gate oxide was grown in a dry O_2 ambient at 1150 ºC for 180 min, resulting in a thick SiO_2 layer. In all other respects the thin-SiO_2 and thick-SiO_2 processes were the same. Figure 5.2 shows microscopic images of the fabricated n-channel MOSFETs using the low thermal budget technique.

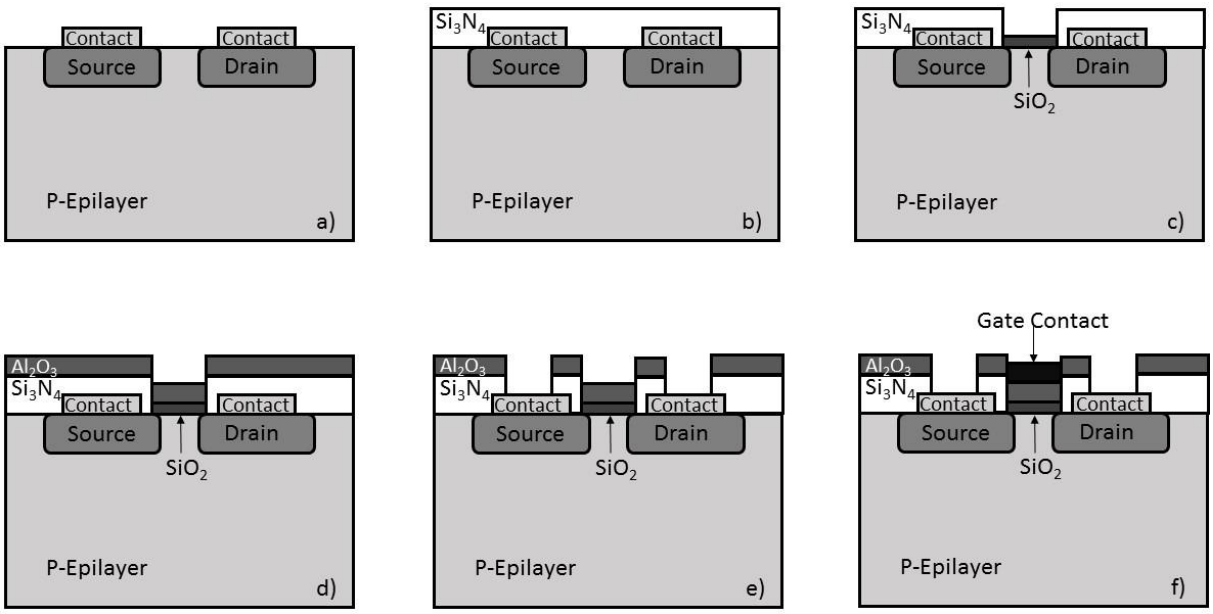


Figure 5.1: Schematic flow chart of the fabrication process of MOSFETs devices with gate oxide grown at low temperature.

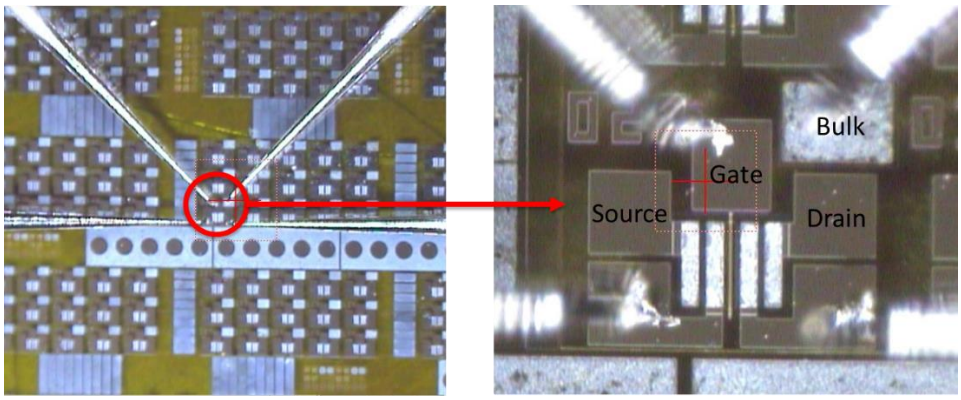


Figure 5.2: Microscopic images of fabricated n-channel MOSFETs using the low thermal budget technique.

5.3 Ion Implantation

Prior to gate oxide formation, all samples were patterned to implant the source and drain with N impurities to form an n-type region via ion implantation. Multi-energy steps were used to form a box doping profile with a doping concentration 4.7×10^{19} cm^{-3} and depth of 100 nm as shown in Table 5.1. The implantation was performed at room temperature with the ion beam perpendicular to the surface and through a 30 nm thick layer deposited on the samples. The additional Al layer provides an alignment mark which is crucial for the subsequent steps and also allows the implanted nitrogen to accumulate near to the surface thus reducing the possibility of forming a p^- region at the surface. Figure 5.3 shows the distribution of doping

concentration with and without the Al layer, simulated by the TRIM (transport of ions in matter) 2D numerical simulation program, with an energy of 20 keV for the implanted N atoms [141]. Simulations showed high concentrations of implanted ions near to the SiC surface using the additional deposited Al layer. In contrast, N ions were concentrated 50 nm from the surface without the deposited Al. Then, photoresist 2 µm thick was patterned as a mask on the Al. In order to obtain such a thickness, the photoresist was spun at 3500 rpm for 40 s before being baked at 90 °C for 10 min. Finally, the samples were attached to the Si wafer using photoresist and sent for ion implantation at the University of Surrey, UK.

No of step	Energy (keV)	Nitrogen Dose (cm^{-3})
1	80	1.90×10^{14}
2	60	1.30×10^{14}
3	40	8.00×10^{13}
4	30	6.00×10^{13}
5	20	6.50×10^{13}
6	10	5.00×10^{13}
Total		5.75×10^{14}

Table 5.1: Energy and nitrogen dose for ion implantation

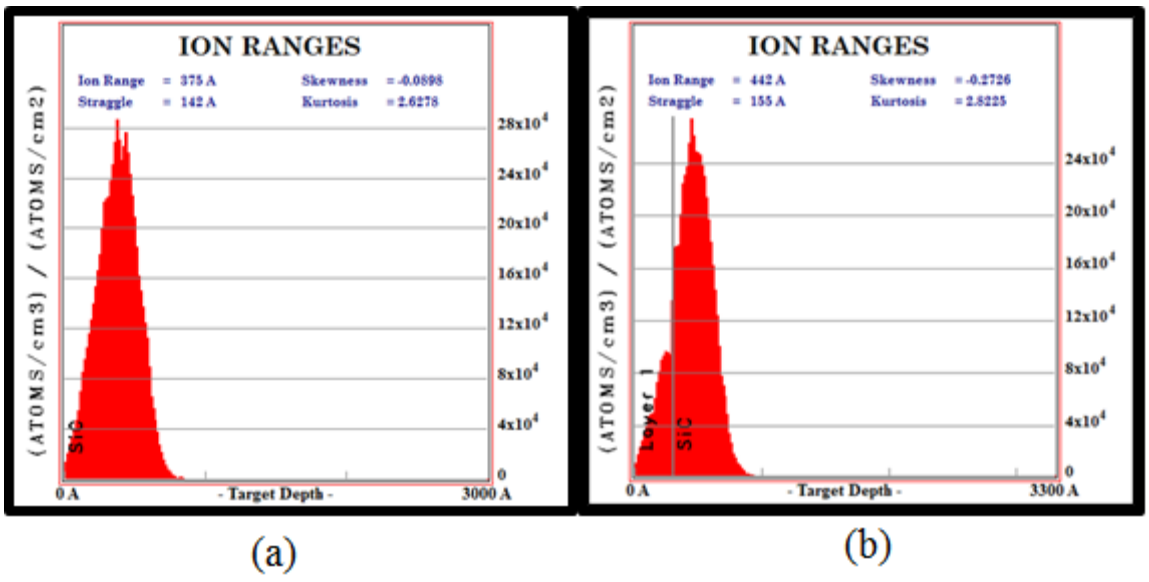


Figure 5.3: Implantation profile of nitrogen ions (a) without and (b) with 30 nm of aluminium layer simulated using (TRIM) 2D numerical program.

To define the implanted doping concentration, SIMS (secondary-ion mass spectrometry) was used. This measurement was used to analyse the composition of the implanted area profile by bombarding the samples with a focused primary ion beam before collecting the ejected secondary ions. Figure 5.4 depicts the area of sputtered samples observed using an optical profilometer. Figure 5.5 shows doping concentration as a function of depth profile extracted from the secondary ions analysed by SIMS. An excellent box shape of the doping profile with a depth of 100 nm was obtained with a high concentration of nitrogen ions near to the surface attributed to using the deposited Al layer. This implies that the source and drain were successfully implanted with a high doping concentration, $N_A = 4.7 \times 10^{19}$ cm^{-3} near to the surface.

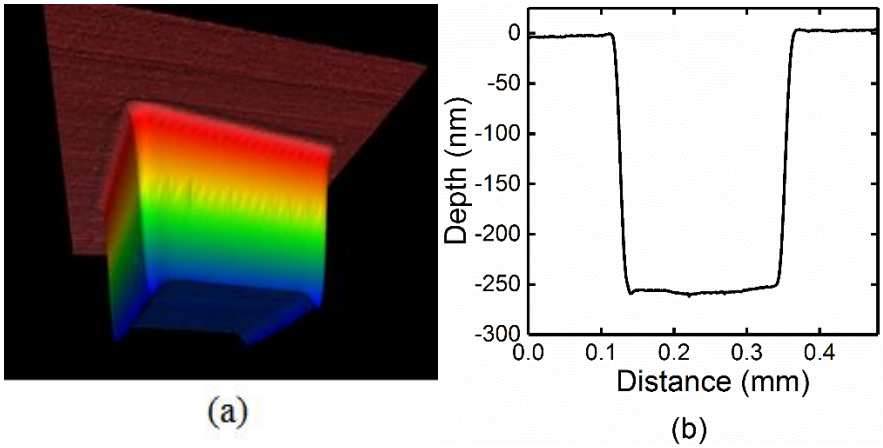


Figure 5.4: Implanted region (a) 3-D image and (b) depth profile measured using optical profilometer.

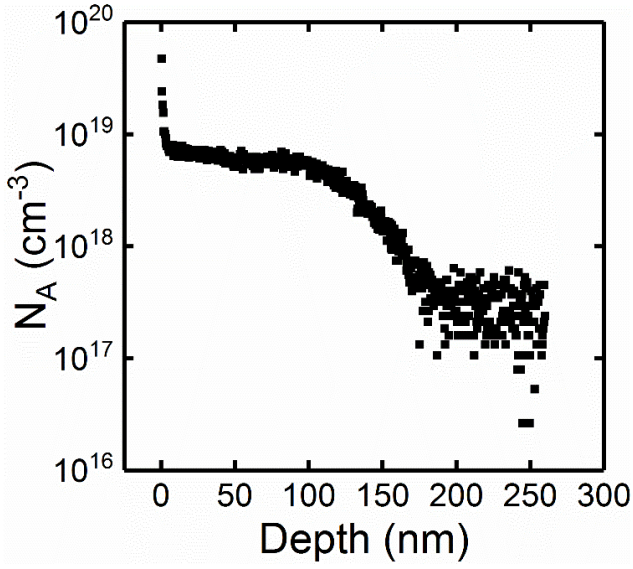


Figure 5.5: Depth profiles of doping concentration by SIMS.

5.4 Post-Implantation Annealing

After the ion implantation process, samples received a post-implantation annealing to activate the implanted impurities. Prior to the exposure to high temperature annealing, a layer of graphite known as a carbon cap was formed with AZ-5214 photoresist. This layer was spun at 4400 rpm for 40 s using a spinner to obtain a uniform thickness. Then samples were baked at 90 °C for 7 min followed by blank exposure to the whole surface for 12 s. Next, a multi-step post-bake was employed at temperatures of 130 °C and 160 °C for 30 min each then at 200 °C for 60 min, resulting in a layer thickness of 1.4 µm. Finally, samples were heated up to 800 °C for 40 min in vacuum using an Edwards 306 coater to complete the formation of the graphite layer. This graphite layer was used to protect the surface during post-implantation annealing and also to avoid the out-diffusion of the dopants [7, 140, 142, 143].

Next, the post-implantation annealing process was performed in a J.I.P.ELEC. SiC furnace specially developed for high temperature processes. Samples were placed in a special crucible which consisted of a SiC-coated graphite susceptor and cap during this process. A fast heating ramp of about 50 °C/s was applied to the crucible by RF heating. Samples were annealed at 1700 °C for 10 min under atmospheric pressure with argon flow in a quartz chamber, which had previously been purged and pumped out below 10^{-3} Torr [140]. After the annealing process, the capping layer has to be removed before gate oxide formation. Several methods were investigated in order to obtain minimum surface roughness after the removal of the capping layer above the channel region with the low thermal budget approach to minimize any possibility of SiC surface oxidation. It is well established that higher surface roughness may contribute to lower channel mobility in MOSFETs [12]. The graphite layer was then removed by plasma asher, reactive ion etching (RIE) and oxidation in the furnace. After that, all samples were cleaned using the standard cleaning process of the Radio Corporation of America (RCA) procedure before being characterised by Raman spectroscopy and Atomic Force Microscopy (AFM).

5.4.1 Plasma asher

Typically, a plasma asher is used to clean organic compounds such as residual photoresist from the surface of the sample. By utilizing the plasma source, a reactive species of single oxygen (O) atoms is created and this reactive species bombards organic compounds on the sample to form a kind of ash before removal using a vacuum pump. In this research, the plasma asher process named the Tegal PLASMOD 100 W Tabletop Plasma Reactor was exploited as a

method to remove the carbon cap layer. The samples were placed in the plasma asher with a variation in timeframe from 30 min to 150 min while maintaining the RF power at room temperature.

Figure 5.6 shows the Raman spectra of the 4H-SiC before and after plasma etching for 90 min. Double sharp mode peaks around 1600 cm^{-1} and 1350 cm^{-1} were detected on the samples with the carbon cap. These peaks are known as G (graphitic) and D (disorder) Raman bands and are generally detected in the spectra of amorphous C materials and are indicative of the graphite nanocrystalline structure [140, 144]. Samples experienced plasma etching for 30, 60, 90 and 150 min at room temperature. The C-related peaks started to disappear only after 90 min of plasma exposure which corresponds to complete carbon cap removal. Figure 5.7 shows AFM images after the carbon cap removal by plasma etching for (a) 90 min and (b) 150 min followed by RCA cleaning. RMS values after plasma etching for 90 min and 150 min are 0.46 nm and 0.50 nm respectively, indicating relatively low surface roughness compared with the bare SiC sample with an RMS = 0.45 nm. Hence plasma etching removed the carbon cap effectively after 90 min of exposure leaving very good surface quality but the RMS increased with increasing timeframe.

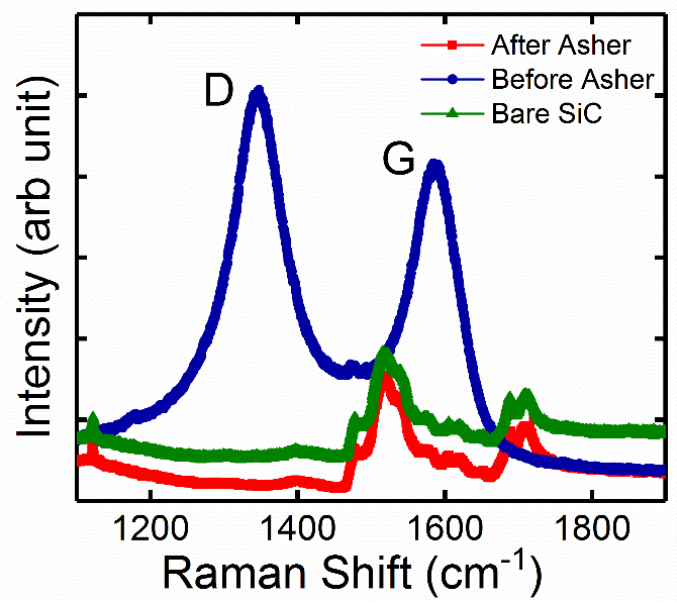


Figure 5.6: Raman spectra before and after plasma etching for 90 min on 4H-SiC.

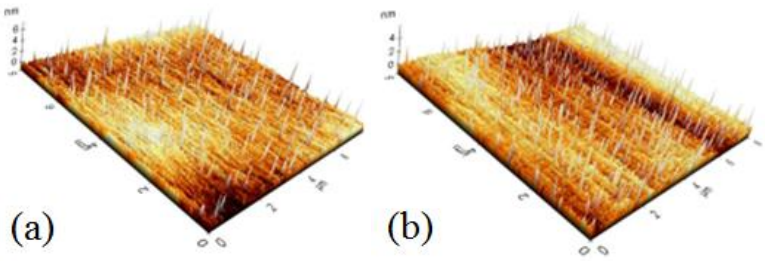


Figure 5.7: AFM images after carbon cap removal using plasma etching for (a) 90 min and (b) 150 min on 4H-SiC.

5.4.2 Furnace oxidation

Oxidation at low temperatures between 700 - 950 °C in the furnace followed by BHF etching cleaning is the standard method to remove the carbon cap [7, 140, 142, 143]. Conceptually, the C atom is oxidised by thermal oxidation, thus removing the graphite capping layer. In this research, oxidation was performed at 600 °C for 120 min and 240 min as well as at 900 °C for 240 min. Based on the Raman spectroscopy results shown in Figure 5.8, the carbon caps were completely removed in all cases. Figure 5.9 shows AFM images after carbon cap removal by oxidation at 600 °C for 120 min, at 600 °C for 240 min and at 900 °C for 240 min resulting in RMS values of 0.55 nm, 0.74 nm and 0.77 nm respectively. This indicates that, after carbon cap removal the surface roughness increased with oxidation temperature and time. The values of RMS are higher than those found using the plasma etching removal technique.

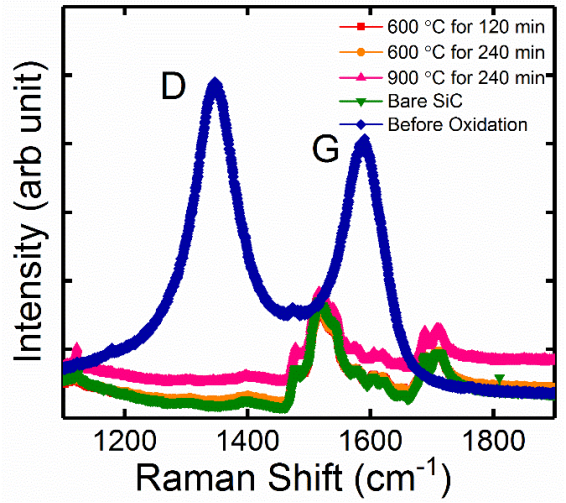


Figure 5.8: Raman spectra after carbon cap removal from 4H-SiC by furnace oxidation. The carbon cap and bare SiC spectra are also shown for comparison.

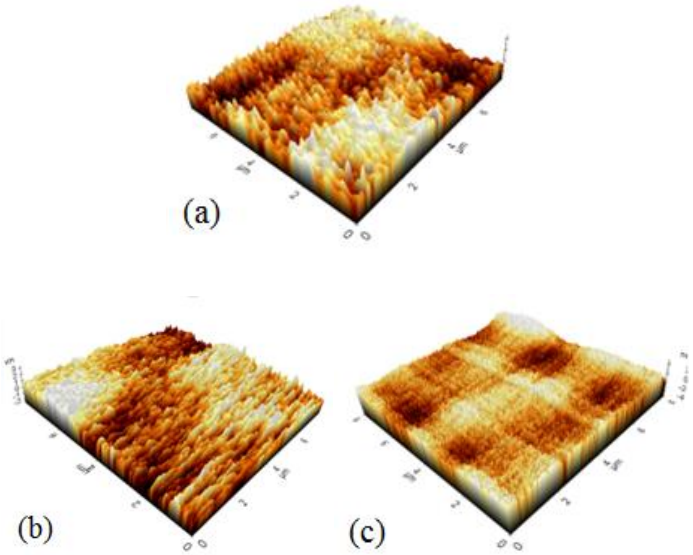


Figure 5.9: AFM images after carbon cap removal by oxidation at (a) 600 °C for 120 min (b) 600 °C for 240 min and (c) 900 °C for 240 min.

5.4.3 Reactive ion etching

Reactive ion etching (RIE) is another approach used to remove the graphite layer [145, 146]. In this study, the samples were etched for a range of durations from 3 to 6 min in the chamber with O_2 gas pumped at 10 sccm. The chamber pressure was set to 20 mTorr with a radio frequency (RF) power of 100 Watt. The reduction in C atom peak intensity (D and G) is directly proportional to time duration as shown in Figure 5.10(a). The carbon cap was completely removed after the RIE process for 6 min. Nevertheless, the surface roughness after 6 min of the RIE process exhibits an RMS value of 2.64 nm which is relatively high compared to that of the bare SiC sample of 0.45 nm resulting from AFM scanning as shown in Figure 5.10(b).

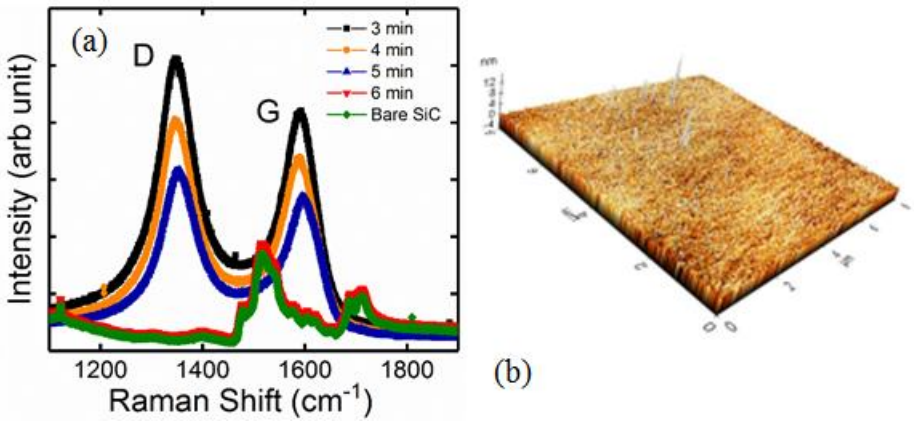


Figure 5.10: Carbon cap removal using RIE method (a) Raman spectra of all analysed samples and (b) AFM image after 6 min of the RIE process.

The appropriate method to remove the carbon cap is determined according to temperature, surface roughness and effectiveness. As a result, carbon cap removal using a plasma asher for 90 min at room temperature is the most suitable and reliable method owing to its effectiveness, low RMS value and lack of any thermal exposure. Thus, this method is used in this research. Furnace oxidation is avoided due to the fact that it involves a thermal process. The RIE technique is not suitable due to the higher RMS value generated after this process. Table 5.2 shows a summary of the parameters of carbon cap removal process parameter and extracted surface roughness values measured by RMS.

Removal method	Temperature (°C)	Time (min)	Carbon Cap Removal	RMS (nm)
Bare SiC	-	-	-	0.45
Asher	RT	30	No	-
		60	No	-
		90	Yes	0.46
		150	Yes	0.50
Furnace	600	120	Yes	0.55
		240	Yes	0.74
	900	240	Yes	0.77
RIE	RT	3	No	-
		4	No	-
		5	No	-
		6	Yes	2.64

Table 5.2: Carbon cap removal process parameter and extracted RMS values

5.5 Device Electrical Characterisation

Electrical characterisation in this chapter was performed using the Agilent B1500A semiconductor device parameter analyser. All MOSFET devices studied have a gate width (W) of 100 µm, while gate length (L) is 2 µm.

Figure 5.11(a) shows the transfer characteristics, i.e. drain current (I_D) as a function of gate overdrive (V_{GS} - V_{th}) measured at room temperature for the fabricated n-channel thin-SiO_2 and thick-SiO_2 MOSFETs. The threshold voltage (V_{th}) is taken to be gate-to-source voltage (V_{GS}) when $I_D = 10^{-10}$ A/µm. Values of SS were extracted from plots of I_D versus V_{GS}

in the subthreshold region where $10^{-11} > I_D > 10^{-12}$ A/μm. For devices having a thick-SiO_2 gate oxide, V_{th} = 4.9 V, along with a large value for SS = 550 mV/dec. But using the thin-SiO_2 gate oxide, SS = 130 mV/dec, which indicates a lower density of charged defects in the vicinity of the channel, while the MOSFET remains as a normally-off device with V_{th} = 2 V. Figure 5.11 (b) shows the corresponding I_D versus V_{DS} relationships for the same devices. The family of curves with increasing V_{GS}-V_{th} for the thin-SiO_2 devices are indicative of good electrostatic control. Figure 5.11(b) also includes a single I_D-V_{DS} curve for a thick-SiO_2 device, where V_{GS}-V_{th} = 5 V. Figure 5.11 illustrates the difference in current drive capability for thick-SiO_2 and thin-SiO_2 devices. There is a major improvement in drain current for the thin-SiO_2 MOSFETs compared with thick-SiO_2 MOSFETs for the equivalent gate overdrive voltage (V_{GS}-V_{th}). This is further clarified in Figure 5.12, which is a plot of the ratio I_D (thin-SiO_2) / I_D (thick-SiO_2) as a function of V_{GS}-V_{th}. This current ratio peaks at 120 for a gate overdrive voltage of 1.7 V, while at 5 V the current ratio is 35. This large current ratio between the gate oxides could be ascribed to the excellent quality of the thin-SiO_2 gate oxide/SiC interface.

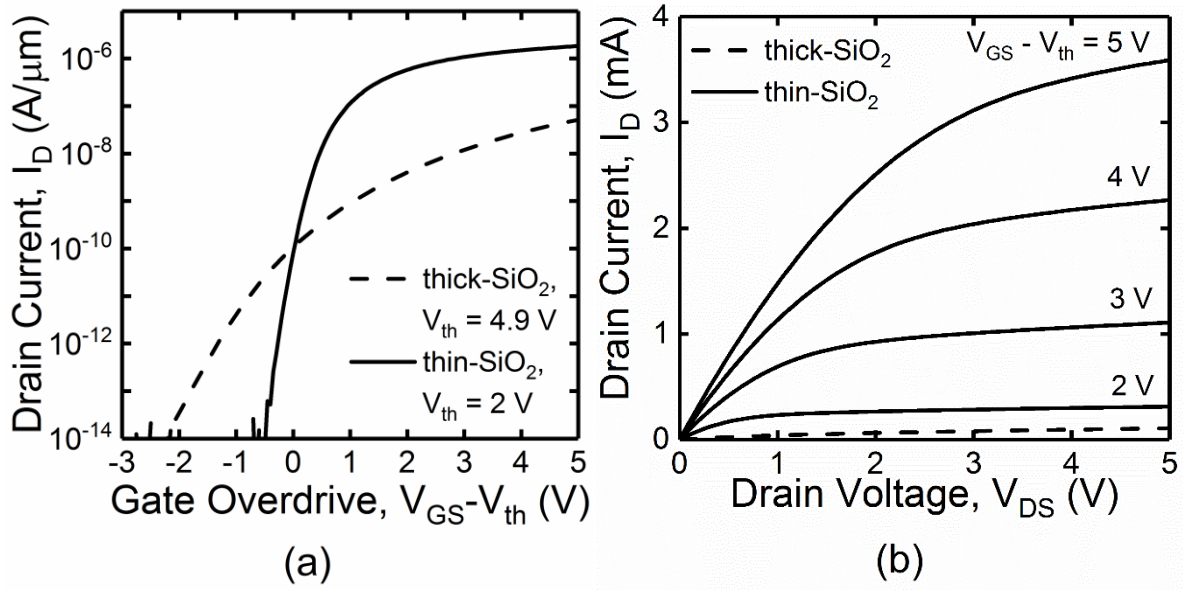


Figure 5.11: Thin-SiO_2 and thick-SiO_2 MOSFETs (a) Transfer characteristic I_D versus (V_{GS}-V_{th}) and (b) Output characteristic I_D versus V_{DS}.

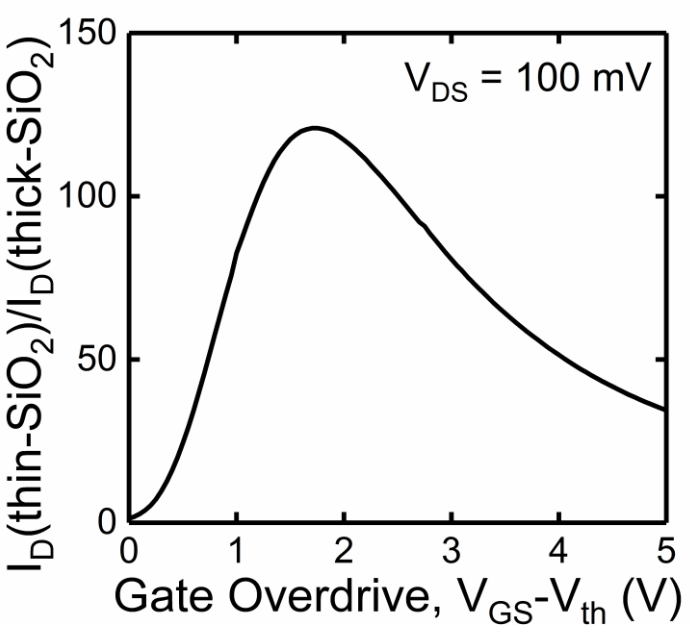


Figure 5.12: I_D ratio of thin-SiO_2/thick-SiO_2 as a function of gate overdrive (V_{GS}-V_{th}).

5.6 Gate Oxide Densification

A previously recognised concern relating to the use of a high-k dielectric material such as Al_2O_3 in the gate stack is the hysteresis in I_D versus V_{GS}, which arises through the trapping and de-trapping of electrons in the oxide as the gate voltage is swept [126]. O vacancies have 5 stable charge states in the Al_2O_3 energy bandgap. The change in trapped charge in the oxide leads to a threshold voltage shift corresponding with the hysteresis. This effect can be reduced by the densification of the deposited Al_2O_3 layer using a low temperature anneal. Temperatures in the range 150 ºC to 400 ºC were investigated to optimise this anneal. Figure 5.13 indicates the variation in threshold voltage hysteresis (ΔV_{th}) over a wide range of anneal temperatures for 60 min on thin-SiO_2 devices. Each point of the ΔV_{th} value is the average from 5 different devices. Voltage hysteresis values as low as 0.7 V were found at anneal temperatures of 250 and 300 ℃ for 60 min. When the anneal temperatures increased above 300 ℃, the values of ΔV_{th} increases. We expect this behavior to be the result of noise due to the large error during high temperature measurement. Measurements were performed at room temperature after the annealing process.

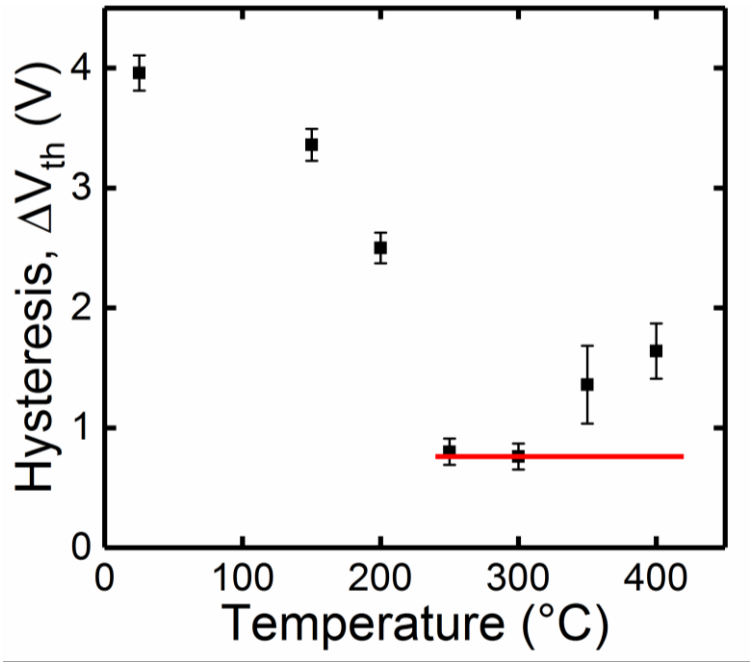


Figure 5.13: Change in threshold voltage hysteresis (ΔV_{th}) measured at room temperature against an anneal temperature for 60 min on thin-SiO_2 devices.

The reduction in voltage hysteresis is shown in Figure 5.14 (a), changing from 4 V for the as-deposited Al_2O_3 film to 0.7 V following an anneal at 300 ºC for 60 min corresponding with a reduction in trapping and de-trapping of charges in the oxide. The residual hysteresis in I_D versus V_{GS} following the 300 ºC anneal, although much reduced, is larger than that found in MOSFETs fabricated using the thick-SiO_2 process, which is 0.2 V as depicted in Figure 5.14(b). This indicates that further improvements in reducing the hysteresis may be possible.

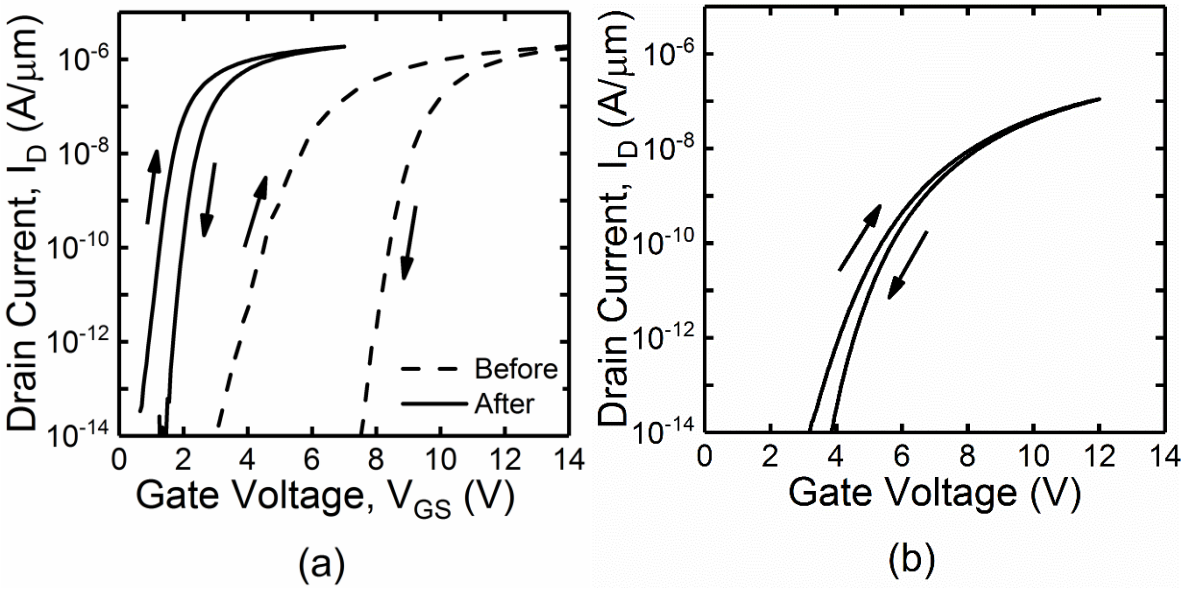


Figure 5.14: I_D vs V_{GS} hysteresis (a) Impact of annealing for thin-SiO_2 compared to (b) thick-SiO_2 device.

5.7 Field Effect Mobility

The field effect mobility, μ_{FE} was determined using equation 5.1 [84].

$$\mu_{FE} = \frac{Lg_m^i}{WC_{ox}V_{DS}} \tag{5.1}$$

where g^i_m is the intrinsic transconductance [147], V_{DS} is the source-drain voltage (V_{DS} = 100 mV) and C_{ox} is the oxide capacitance per unit area of the MOSFETs measured using a split C-V configuration.

High electron mobility was obtained for SiC MOSFETs fabricated using the thin-SiO_2 process. Figure 5.15 shows a plot of field effect mobility versus effective electric field in the SiC close to the dielectric interface, E_{eff}. Since E_{eff} is a function of V_{GS}, the gate overdrive voltage is also indicated on the same graph. E_{eff} in the gate dielectric and SiC can be expressed as in equations 5.2 and 5.3 [92].

$$E_{eff}(\text{dielectric}) = \frac{1}{\varepsilon_{SiO_2}}(Q_B + Q_N) \tag{5.2}$$

$$E_{eff}(\text{SiC}) = \frac{1}{\varepsilon_{SiC}}\left(Q_B + \frac{1}{2}Q_N\right) \tag{5.3}$$

where Q_B and Q_N are the charge layer densities in the depletion and inversion layers respectively which and can be determined as below:

$$Q_B = \sqrt{2\varepsilon_{SiC}qN_A(2\psi_B)} \tag{5.4}$$

$$Q_N = (V_{GS} - V_{th})C_{ox} \tag{5.5}$$

It can be seen that the mobility peaks at 125 $cm^2/V.s$ for a gate overdrive of 4 V and an effective electric field, E_{eff}, of 0.35 MV/cm. Mobility remains above 120 $cm^2/V.s$ up to a gate overdrive of 6 V, corresponding to an effective electric field in the SiC of 0.49 MV/cm and an effective electric field in the gate dielectric of 2.2 MV/cm. Mobility will decrease for higher values of E_{eff}, but only drops by 25% of its peak value for a gate overdrive of 8 V, corresponding to E_{eff} = 0.6 MV/cm and an effective electric field in the gate dielectric as high as 3 MV/cm.

The mobility in the thin-SiO_2 device is much higher than that in the thick-SiO_2 (control) device, where the peak mobility is only 7 $cm^2/V{\cdot}s$, corresponding to an enhancement factor of

18× in peak mobility using thin-SiO_2. Figure 5.15 represents the best measured mobility, but high mobilities were obtained in all working devices using the thin-SiO_2 process, with many in excess of 100 $cm^2/V{\cdot}s$.

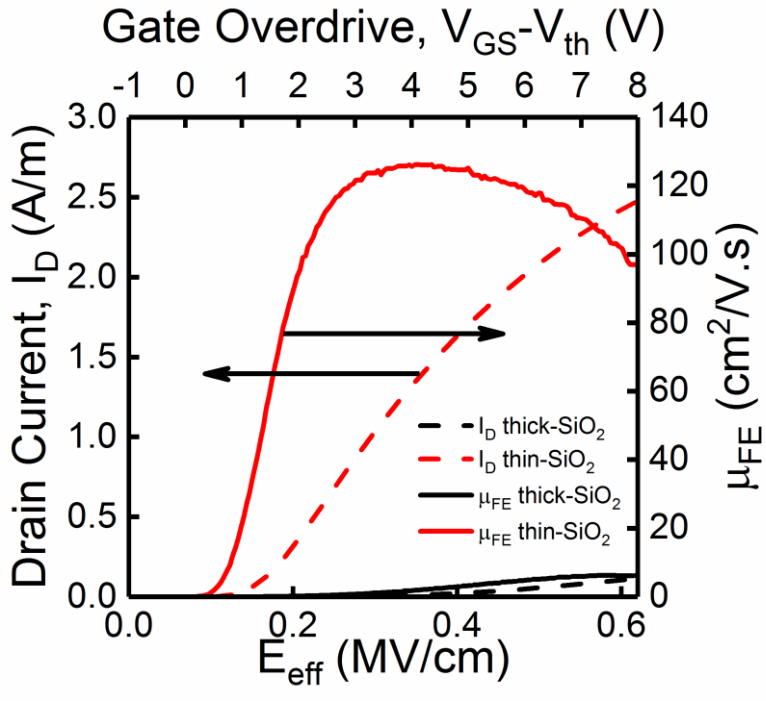


Figure 5.15: μ_{FE} and corresponding I_D of fabricated MOSFETs as a function of gate overdrive and E_{eff} in SiC

5.8 Correlation of Field Effect Mobility with Density of Interface Traps (D_{it})

It is well known that interface traps are the origin of Coulombic scattering, which affects the electron mobility in the channel of MOSFETs [12]. Figure 5.16 shows D_{it} as a function of energy in relation to the valence band maximum ($E - E_v$) obtained from both p-type (valence band edge) and n-type (conduction band edge) MOS capacitors. D_{it} levels in the range from 6×10^{11} - 5×10^{10} $cm^{-2}.eV^{-1}$ were found when the thin-SiO_2 process was used to fabricate MOS capacitors. This represents a reduction in D_{it} by 1-2 orders of magnitude compared to MOS capacitors fabricated with the thick-SiO_2 process. This suggests that D_{it} is inversely proportional to channel mobility, which is in agreement with a theoretical study [12] and previous reports [7, 46]. Details of the behaviour of these MOS capacitors have been discussed in chapter 4.

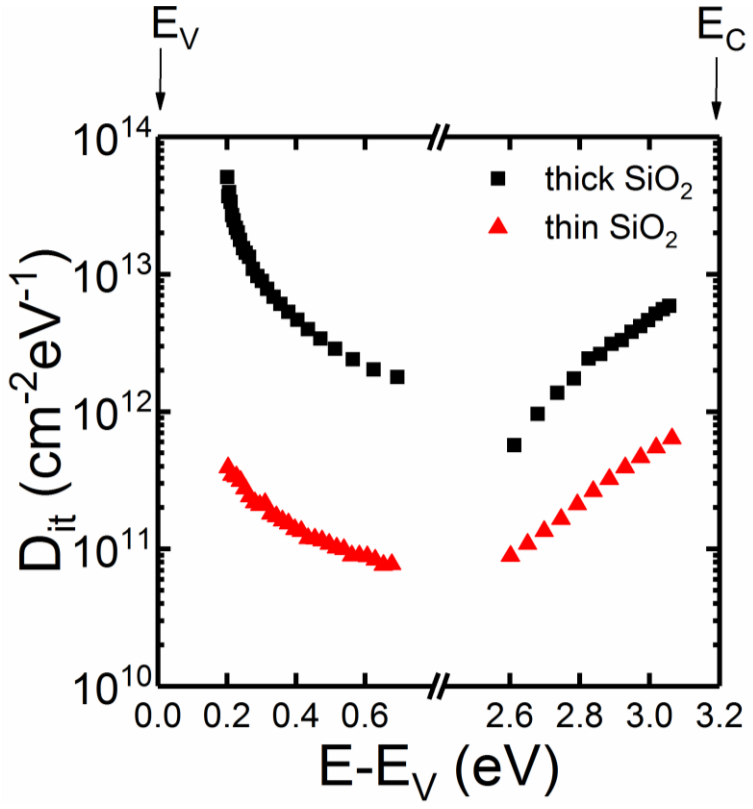


Figure 5.16: Distribution of D_{it} near the valence and conduction band edges

5.9 High Temperature Measurement

As SiC is a wide bandgap semiconductor, 4H-SiC devices have a well-recognised ability to operate in hostile environments such as at high temperatures. Thus, demonstrating good performance of MOS devices under such conditions is required to accomplish the objective of this study. High temperature measurements up to 300 °C were performed on both thin-SiO_2 and thick-SiO_2 devices to study effects on electrical characteristics for each device. Figure 5.17 shows I_D - V_{GS} characteristics for (a) thin-SiO_2 and (b) thick-SiO_2 MOSFETs at elevated temperature. Subthreshold current (I_{Sub}), V_{th} and saturated drain current changed with increasing temperature due to several factors discussed below. The I_{Sub} for both devices increased with increasing temperature but can still be considered small. This is attributed to the high quality of the gate oxide formed on both devices.

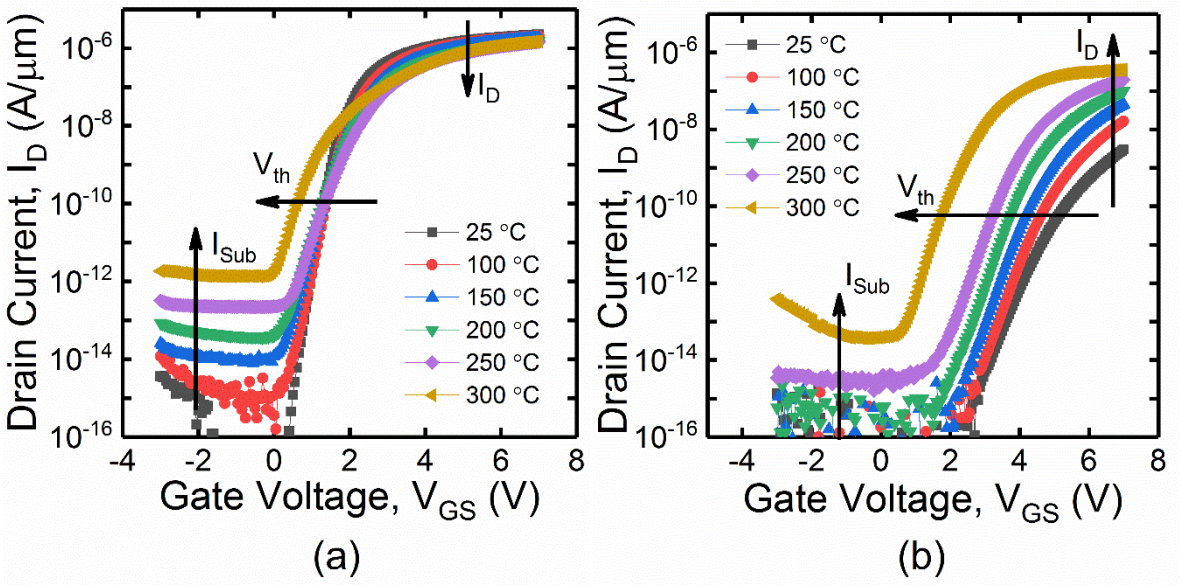


Figure 5.17: I_D - V_{GS} characteristics at elevated temperature for (a) thin-SiO_2 and (b) thick-SiO_2 MOSFETs

5.9.1 Threshold voltage vs temperature

The stability of the V_{th} in high temperature conditions is a major concern determining the device performance. The ability to operate as a normally off device or in enhancement mode where the device is off at zero V_{GS} is necessary.

Figure 5.18 shows the V_{th} change against temperature during the (a) forward sweep and (b) reverse sweep for both devices. Each point of the V_{th} value is the average from 5 different devices. Devices with gate oxide having a thick-SiO_2 exhibit a gradual reduction of V_{th} from approximately 5 V at room temperature to 2 V and 3 V for forward and reverse sweeps respectively at 300 °C. Similar trends could be seen for the forward sweep in thin-SiO_2 devices. A slightly decreased value of V_{th} in thin-SiO_2 devices occurred with increasing temperature from 2 V at 25 °C to 0.4 V at 300 °C. In contrast, values of V_{th} increased with measured temperature and peaked at 250 °C with V_{th} = 3.1 V before dropping to 1.9 V at 300 °C. Overall, both devices demonstrated a fall with increasing temperature up to 300 °C and this is in agreement with theoretical calculations [12] and previous reports [93, 148]. This suggests that thin-SiO_2 devices could retain normally-off device behaviour at high temperatures as high as at 300 °C and this indicates their capability to be operated at high temperature.

Corresponding to the different V_{th} values of both sweeps, ΔV_{th} against elevated temperature is shown in Figure 5.19. Devices fabricated with the thin-SiO_2 process showed a

fluctuation in ΔV_{th} over a wide range of measured temperature. Each point of the ΔV_{th} value is the average from 5 different devices. Values of ΔV_{th} less than 1 V were obtained at the measured temperatures of 25 and 100 °C before significantly increasing with further increase in temperature and peaking at 200 °C at ΔV_{th} = 1.7 V. In contrast, consistent ΔV_{th} for thick-SiO_2 gate oxide with values less than 0.5 V were observed up to 250 °C before increasing to 0.7 V at 300 °C. Nevertheless, the ΔV_{th} values of thin-SiO_2 gate oxide are still greater than those found in MOSFETs fabricated with the thick-SiO_2 process. The nature of the Al_2O_3 layer, which contains of 5 stable charges of O vacancy, could explain this behaviour in thin-SiO_2 devices [126]. As the voltage is swept, electron trapping and de-trapping in the oxide occurred and this corresponds to the hysteresis observed in Figure 5.19.

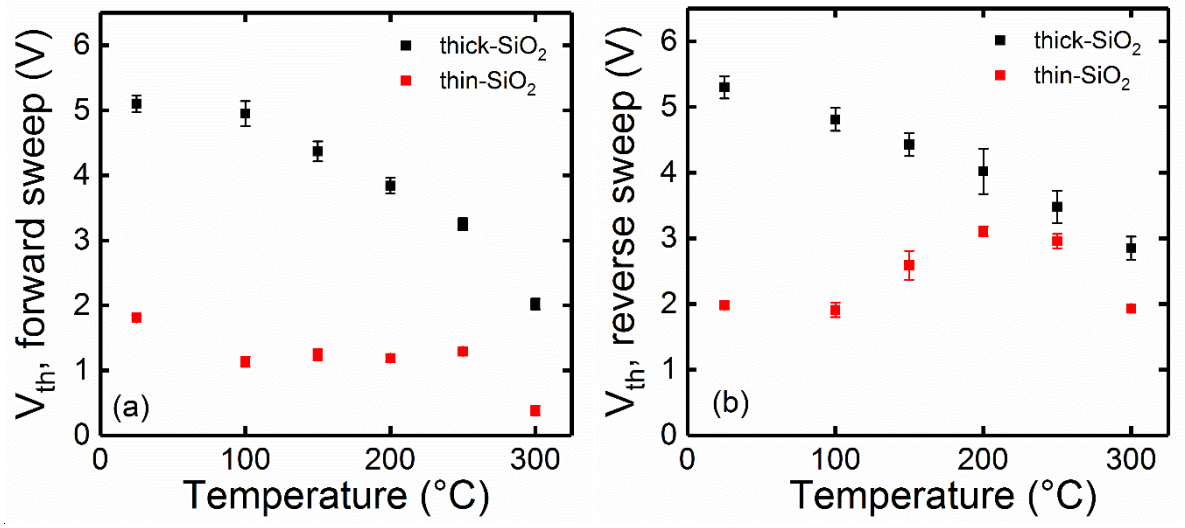


Figure 5.18: Threshold voltage during (a) forward sweep and (b) reverse sweep as a function of temperature

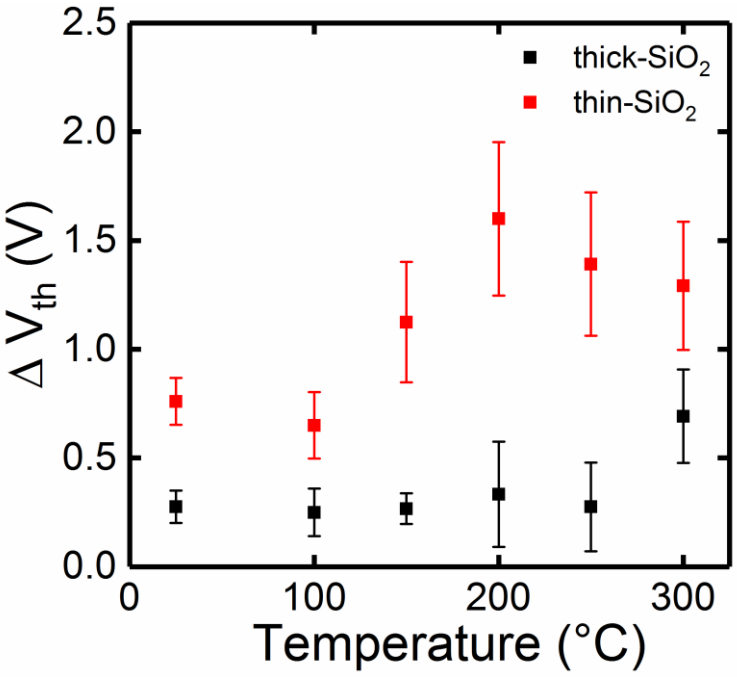


Figure 5.19: Threshold voltage hysteresis versus temperature for both fabricated devices

5.9.2 Field effect mobility vs temperature

In order to investigate the mechanism of electron transport, field effect mobility trends in thin-SiO_2 and thick-SiO_2 devices were observed at elevated temperature. Based on Matthiessen's rule which is well accepted for thick oxide Si technology, several factors limit electron mobility. The three major factors as mentioned in section 3.3.4 are Coulombic scattering, phonon scattering and surface roughness. To determine which factors most limit electron mobility, high temperature measurements were performed since most of these factors are temperature-dependent [7]. Powell *et al.* [94] suggested that phonon mobility are reduced with increasing temperature, whereas Coulombic mobility increases. Meanwhile, the effect of surface roughness on mobility is not affected by temperature. Thus, if the field effect mobility increases with temperature, then the limiting factor is Coulombic scattering (interaction time reduces). In contrast, if field effect mobility decreases with increasing temperature, it is dominated by the phonon scattering (greater lattice vibration). Figure 5.20 shows the peak field effect mobility of thin-SiO_2 decreasing with temperature from 125 $cm^2/V.s$ at room temperature to approximately 72 $cm^2/V.s$ at 300 °C measured from 5 different devices. This represents a drop in peak field effect mobility by 40% compared to its value at room temperature, which suggests that the devices operational capability is intact even high temperatures. This reduction also indicates that phonon scattering governs electron mobility in thin-SiO_2 devices rather than

Coulombic scattering. The density of interface traps is believed to be the major factor associated with Coulombic scattering [7, 94]. This is consistent with our earlier finding that the thin-SiO_2 MOS capacitors demonstrate low values of D_{it} of 6.0×10^{11} $cm^{-2}.eV^{-1}$ at 0.2 eV below the conduction band edge as outlined in section 4.3.5. Contrarily, the μ_{FE} for thick-SiO_2 devices increases with temperature from around 7 $cm^2/V.s$ at 25 °C up to 28 $cm^2/V.s$ at 300 °C, measured from 5 different devices. This increase represents a clear indication that electron mobility in thick-SiO_2 devices is controlled by Coulombic scattering as has been discussed in section 3.3.4.

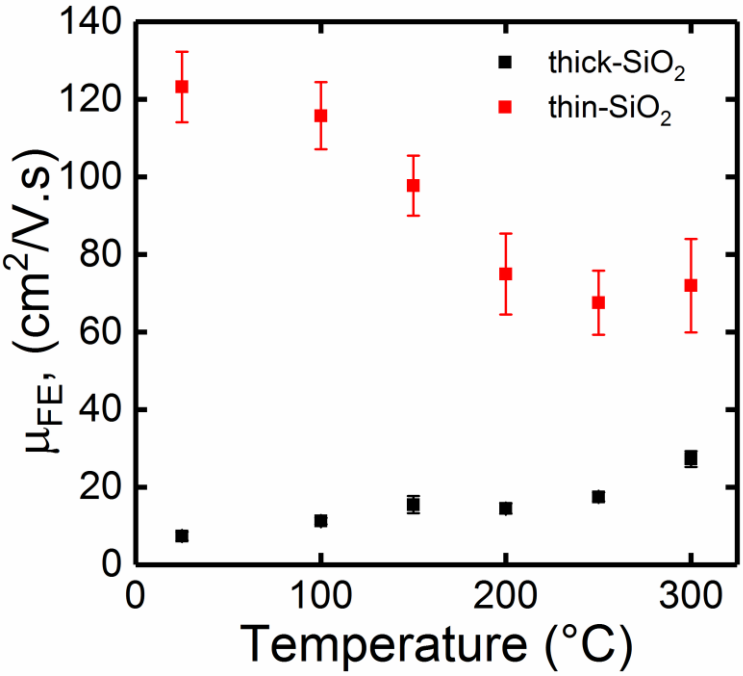


Figure 5.20: Peak field effect mobility as a function of measurement temperature

5.9.3 Subthreshold slope vs temperature

The SS indicates the device's transition rate from the off state (low current) to the on state (high current) and is an important feature in MOSFETs. Figure 5.21 shows the change in SS against temperature for MOSFETs fabricated with thin-SiO_2 and thick-SiO_2 gate oxides. Each point of the SS value is the average from 5 different devices. The SS value was extracted from the I_D-V_{GS} curve extracted in the subthreshold region where $10^{-11} > I_D > 10^{-12}$ A/μm. Ideal SS as a function of temperature is defined in equation 5.6 and also included for comparison.

$$SS = \frac{kT}{q}\ln(10) \tag{5.6}$$

MOSFETs having thin-SiO_2 gate oxides display an SS values of 127 mV/dec at room temperature. As the measured temperature increases, SS values for thin-SiO_2 devices increase steadily to 391 mV/dec at 300 °C. This represent an increase of more than threefold in the subthreshold slope with increasing temperature. The increment in SS values with increasing temperature was expected as plotted of ideal SS values of thin-SiO_2 devices, since the value of SS is directly proportional to kT/q as given equation 5.7. The increase of SS value with increasing temperature only valid if the concentration of interface traps are relatively low.

$$SS = \ln(10)\frac{kT}{q}\left(\frac{C_{ox}+C_D+C_{it}}{C_{ox}}\right) \tag{5.7}$$

where $C_{ox,}$ C_D and C_{it} are oxide capacitance, depletion capacitance and the interface trap capacitance of the device respectively [12].

In contrast, thick-SiO_2 gate oxide devices exhibit a reduction in SS against increasing temperature. SS values of 590 mV/dec were obtained at room temperature and these gradually decreased with increasing temperature. As the measured temperature reached 300 °C, an SS value of 365 mV/dec was recorded. This reduction suggests that the values of SS of MOSFETs having a thick-SiO_2 gate oxide were possibly affected by high concentrations of interface traps, as the trapped electrons are released and easily become excited at higher temperature. It is well-known that interface traps are the source of Coulombic scattering [7, 12, 69]. Results for the MOS capacitor described in section 4.3.6 show that D_{it} in thick-SiO_2 gate oxide devices were relatively high and decreased with increasing temperature. This reduction trend in D_{it} may be attributed to the SS reduction with increasing temperature for thick-SiO_2 MOSFETs. This correlation is given in equation 5.7. The SS trend against elevated temperature for thin-SiO_2 proves our earlier findings in chapter 4 that values of D_{it} in thin-SiO_2 devices have been successfully reduced and have less impact on current conduction in the subthreshold region. On the other hand, thick-SiO_2 gate oxide devices generate large concentrations of D_{it} which distort the current conduction and thus affect SS values with changes in temperature.

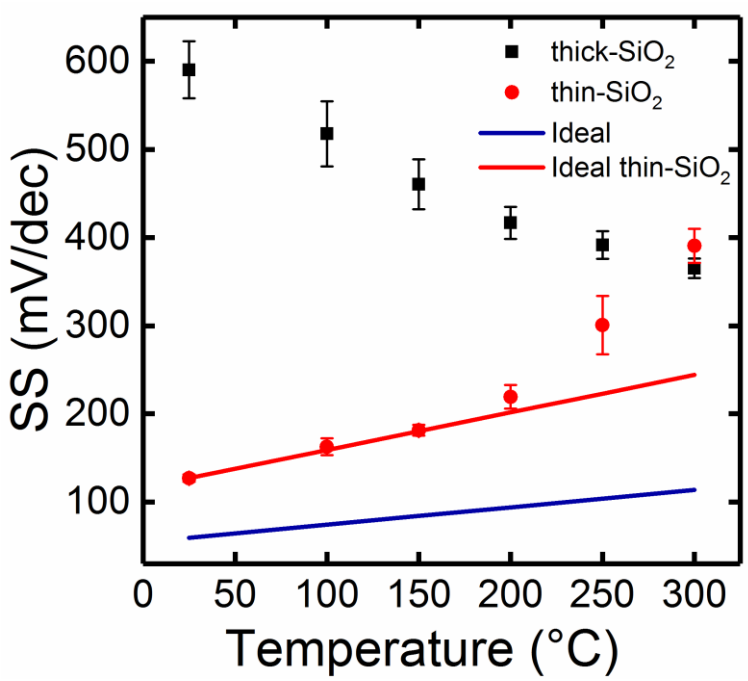


Figure 5.21: Subthreshold slope change for MOSFETs fabricated with thin-SiO_2 and thick-SiO_2 gate oxide as a function of elevated temperature

5.10 Other MOSFETs Fabricated Using Low Thermal Budget Technique

In addition to thin-SiO_2 gate oxide devices fabricated with oxide growth at 600 °C for 3 min using the low thermal budget technique, several MOSFETs were also fabricated using the same technique but with different oxide growth parameters. Table 5.3 shows the oxidation condition parameters for all fabricated n-channel MOSFETs. These additional oxidation conditions were explored to further verify the best parameters that could produce the highest field effect mobility. The low thermal budget technique was used during oxide growth, where after the ultrathin SiO_2 layer was grown by RTP, an Al_2O_3 layer was deposited over the thin layer to complete the gate stack. For oxide growth at 400 and 500 °C for 3 min, no measurements can be performed due to the high leakage occurring at the gate stack. This suggests that the ultrathin SiO_2 layers had not been adequately formed as a complete layer or were not uniformly grown over the 4H-SiC, and hence the interface quality deteriorated. For MOSFETs having gate oxide grown at 550 °C for 2 min, peak channel mobility as low as 5.5 $cm^2/V.s$ were obtained with a subthreshold slope of 450 mV/dec. As the oxidation temperature increased to 600 °C with a similar time of 2 min, the peak channel mobility increased up to 18.7 $cm^2/V.s$ with a subthreshold slope of 361 mV/dec. The highest peak field effect mobility of 125 $cm^2/V.s$ was obtained with MOSFETs having gate oxide grown at 600 °C for 3 min, with the lowest

subthreshold slope of 127 mV/dec. This MOSFET has been discussed in the early sections of this chapter and is referred to here as "thin-SiO_2". Values of peak channel mobility drop, as the oxidation temperature increases to 42.6 and 23.8 cm^2/V.s for gate oxides grown at 700 °C for 1 min and 800 °C for 3 min respectively. To further investigate the excellent channel mobility that has been shown by gate oxides grown at 600 °C for 3 min, an additional nitridation step was performed. An anneal in N_2O ambient at 850 °C for 1 hr was performed immediately after oxidation. The Al_2O_3 layer was deposited after the nitridation anneal to complete the device gate stack. The nitridation anneal in N_2O was presumed to have created a strong bond between nitrogen atoms with strained or dangling Si atoms at the interface thus passivating the interface traps [42]. However, the peak channel mobility dropped rapidly down to 3.5 cm^2/V.s, which is less than with normal oxidation at 1150 °C for 2 hr (thick-SiO_2), with a relatively large subthreshold slope of 959 mV/dec. The additional nitridation anneal has not effectively increased the channel mobility but has caused the interface quality to deteriorate. This could be explained by the fact that the N_2O anneal has formed a large concentration of C defect after experiencing the thermal annealing process at 850 °C for 1 hr [33, 110]. Threshold voltages hysteresis for all devices showed similar values in a range of 1.11 V to 2.05 V due to similar substrate doping concentrations and more or less the same effective oxide thickness. Figure 5.22 shows a correlation between the extracted values of field effect mobility against subthreshold slope value for all fabricated devices, along with previously reported values [29, 50, 65, 71, 73, 149]. Each point of the μ_{FE} and SS value is the average from 5 different devices. It is clear that peak field effect mobility is indirectly proportional to the subthreshold slope. This suggests that Coulombic scattering which limits current conduction in low electric fields in the subthreshold region also has an impact on peak channel mobility.

Oxidation Temperature (°C)	Oxidation Time (min)	ΔV_{th} (V)	SS (mV/dec)	Peak μ_{FE} (cm^2/V.s)
400	2		Leakage	
500	2		Leakage	
550	2	1.12	450	5.5
600	2	1.33	361	18.7
600	3	1.89	127	124.8
700	1	1.50	253	42.6
800	3	2.05	304	23.8
600 + 850 °C for 1 hr in N_2O	3	1.11	959	3.5

Table 5.3: Oxide growth parameters and extracted threshold voltage, SS and μ_{FE} for all n-channel MOSFETs fabricated using low thermal budget technique.

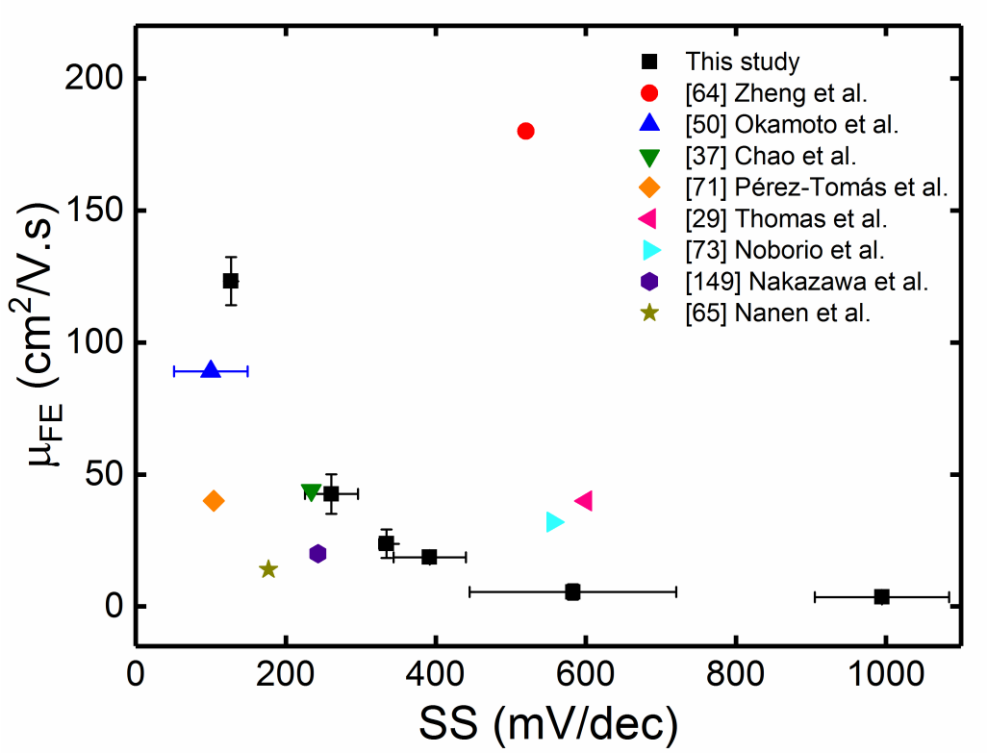


Figure 5.22: Field effect mobility as a function of subthreshold slope for all fabricated devices and previously reported values for Si-face 4H-SiC MOSFETs.

5.11 Key Findings and Conclusion

4H-SiC MOSFETs were successfully fabricated on p-type SiC using a low thermal budget technique. The channel mobility of enhancement mode 4H-SiC devices was increased using a thin-SiO_2 process comprising a 0.7 nm thin SiO_2 layer and Al_2O_3 deposited by ALD to obtain an EOT of 29 nm. MOSFETs fabricated with the same EOT using a thick SiO_2 layer were fabricated alongside for comparison. The quality of the 4H-SiC/oxide interface is improved using the thin-SiO_2 process and in particular defects, resulting from prolonged oxidation, are reduced. These results are consistent with a reduction in C related defects, which has been proposed previously [33]. A peak channel mobility of 125 $cm^2/V{\cdot}s$ was recorded, together with a SS of 130 mV/dec and D_{it} levels in the range from $6{\times}10^{11}$ - $5{\times}10^{10}$ $cm^{-2}.eV^{-1}$, which further indicates good control of charged defects in the 4H-SiC. Remote Coulombic scattering from charges in the deposited Al_2O_3 dielectric is mitigated by a 300 ºC anneal, which also reduces the hysteresis in V_{th} from 4 V to an acceptable value of 0.7 V.

4H-SiC MOSFETs using thin-SiO_2 remained in enhancement mode at elevated temperatures up to 300 °C, indicating that the devices are sufficiently robust to be operated in hostile conditions. The peak channel mobility reduced with increasing temperature, verifying

the notion that the electron conductivity of thin-SiO_2 MOSFETs is limited by phonon scattering. This has overcome Coulombic scattering as a limiting factor of mobility which has been haunting the SiC research community for years. In order to further investigate the oxidation conditions of ultrathin SiO_2 using the low thermal budget technique, several more MOSFETs were fabricated using different oxidation parameters. Oxidation temperatures in a range from 400 °C to 800 °C for durations of 3 min and less were employed to optimise the thin-SiO_2 gate oxide MOSFETs. An additional POA in the nitridation step was also performed on certain devices to increase channel mobility. Among these, those with gate oxide grown at 600 °C for 3 min demonstrated the highest channel mobility with lower SS value. These excellent oxidation parameters are similar to results found for MOS capacitors which have been discussed in chapter 4. The 0.7 nm SiO_2 layer is the thinnest practicable layer for forming a complete bulk SiO_2 [79, 124].

Prior to gate oxide formation, all the MOSFETs were successfully implanted to form the n-region of source and drain. An excellent box shape doping profile was obtained with concentrations as high as $N_A = 4.7 \times 10^{19}$ cm^{-3} near to the surface. The carbon cap which was used to protect the SiC surface during the doping activation process was successfully removed using plasma asher at room temperature. This new technique is critical to keep the thermal budget as low as possible without causing deterioration in surface roughness.

Chapter 6

4H-SiC MOS Capacitor Using Ultrathin Nitrided Oxide Layer with Deposited SiO_2 Gate Stack

6.1 Introduction

Further investigations regarding gate dielectric using an ultrathin SiO_2 layer has been conducted since the success gained from MOS devices, as discussed in chapters 4 and 5. Low values of the density of interface traps (D_{it}) in fabricated MOS capacitors (leading to a higher channel mobility in MOSFETs) have been obtained using the low thermal budget technique. High concentrations of carbon (C) defects, which are believed to be generated during high temperature oxidation have degraded the quality of the oxide/4H-SiC interface [33]. The low thermal budget technique has reduced the generation of C defects and a high channel mobility up to 125 $cm^2/V.s$ has been achieved. However, the use of Al_2O_3 to complete the gate stack has created another problem. The nature of Al_2O_3, which consists of 5 stable charge states of oxygen vacancies, has caused a trapping and de-trapping mechanism to occur [126]. This mechanism is clearly reflected in the hysteresis between forward and reverse sweeps during C-V and I_D-V_{GS} measurements of MOS capacitors and MOSFETs respectively. This behaviour could lead to device instability during operation. Furthermore, this happens not only with Al_2O_3 but all deposited dielectrics including SiO_2 and high k materials [126]. The densification of oxide after deposition via an annealing process is necessary in order to suppress this effect [106, 150, 151]. However, for high k materials, exposure to high temperatures during the post-oxidation annealing (POA) process may transform the oxide structure from being amorphous

to crystalline. High k materials such as HfO_2 start to crystallize at 400 °C [126], ZrO_2 at 700 °C [152] and Al_2O_3 at 800-1100 °C [153-156]. The crystallization of high k material will increase the leakage current and thus degrade device performance [126, 133]. Low temperature POA may be a solution to solve this problem. In section 5.6, we reported that the densification of Al_2O_3 at 300 °C for 60 min reduced voltage sweep hysteresis from 4 V to 0.7 V, but this value is still larger than those found in thermally grown SiO_2, which are less than 0.2 V.

In order to form a gate oxide that could generate low values of D_{it} by means of high electron channel mobility along with less voltage hysteresis, a novel method is proposed. By using deposited SiO_2, the material crystallization effects at high temperature could be avoided due to the fact that SiO_2 is a naturally stable material. In addition, the deposited SiO_2 could withstand electric field up to 10 MV/cm with low leakage current even after POA, as previously reported [129, 157, 158]. An ultrathin layer of SiO_2 which generates less D_{it} and thus increases electron mobility can be grown underneath the deposited SiO_2 layer via annealing in nitrogen (N) rich ambient. This annealing process is widely known to passivate interface traps and improve the quality of the oxide/4H-SiC interface [38, 39, 45, 125]. The N atoms produced by the N-rich gases such as nitrous oxide (N_2O) or nitric oxide (NO) will penetrate underneath the deposited SiO_2 and create a strong bond with dangling Si bonds [42, 43]. At the same time, a thin layer of SiO_2 is grown during the high temperature of N-rich annealing.

This chapter describes the fabrication of n-type 4H-SiC MOS capacitors in a study to obtain a high quality of gate oxide with a low value of D_{it} and a low voltage hysteresis which would compromise device performance and stability. The gate oxide was formed by the deposition of a thick layer of SiO_2 followed by the N-rich annealing process. The high temperature of POA in N-rich ambient will passivate interface traps and at the same time grow an ultrathin layer of SiO_2. The ultrathin SiO_2 layer is the key factor to reduce the value of D_{it} and will further enhance electron mobility. Here it is important to achieve the optimum parameters for ultrathin SiO_2 layer growth, which correlate with deposited SiO_2 layer thickness, N-rich annealing temperature and time. High temperature measurements were performed on the devices that exhibited the lowest D_{it} values to further investigate the stability of the devices during such conditions. The robustness of the gate oxide as well as the current conduction mechanism were also investigated.

6.2 Experimental Details

N-type MOS capacitors with a heavily doped n-type substrate were fabricated on 4° off-axis (0001) Si face, n^+ (sub)/n^+ /n^- (5.5×10^{15} cm^{-3}, 11.3 µm) epitaxial 4H-SiC (0001) wafers supplied by Dow Corning. Firstly, the samples were cleaned by the standard Radio Company of America (RCA) cleaning procedure as shown in Figure 6.1(a). Details of the cleaning process have been described in section 3.5.1. Then SiO_2 was deposited on the samples with a layer thickness of 30 nm or 60 nm using PECVD, as depicted in Figure 6.1(b). This process was performed at 350 °C at a chamber pressure of 1000 mTorr with 20 W of power. After that, the samples experienced a POA in N_2O ambient at 1175 °C for durations in the range of 30-120 min. During this step, the N_2O gas will decompose into NO gas after achieving a temperature of around 700 °C and reacts with the samples. This transformation can be noticed in the change of colour between the furnace and the exhaust flange from colourless at room temperature into brownish as shown in Figure 6.2. This process will cause an ultrathin SiO_2 layer to grow underneath the deposited SiO_2 as shown in Figure 6.1(c). The thickness of the grown SiO_2 layer is estimated using the Deal-Grove model. In addition, MOS capacitors were also fabricated with 30 nm and 60 nm thicknesses of deposited SiO_2 followed by POA performed in N_2 ambient at 1175 °C for 120 min. For comparison, devices with only deposited SiO_2 gate oxide were also fabricated. No POA in N_2O or N_2 was involved in this gate formation process.

Next, 10 nm of Titanium (Ti) as an adhesion layer and 200 nm of Silver (Ag) were deposited onto the top of the device to form the gate contact using an e-beam evaporator as depicted in Figure 6.1(d). Finally, 100 nm of Tungsten (W) was deposited onto the bottom of the device to form the back contact as shown in Figure 6.1(e). Figure 6.3 shows the mask set which was used for the fabrication processes of the MOS capacitors.

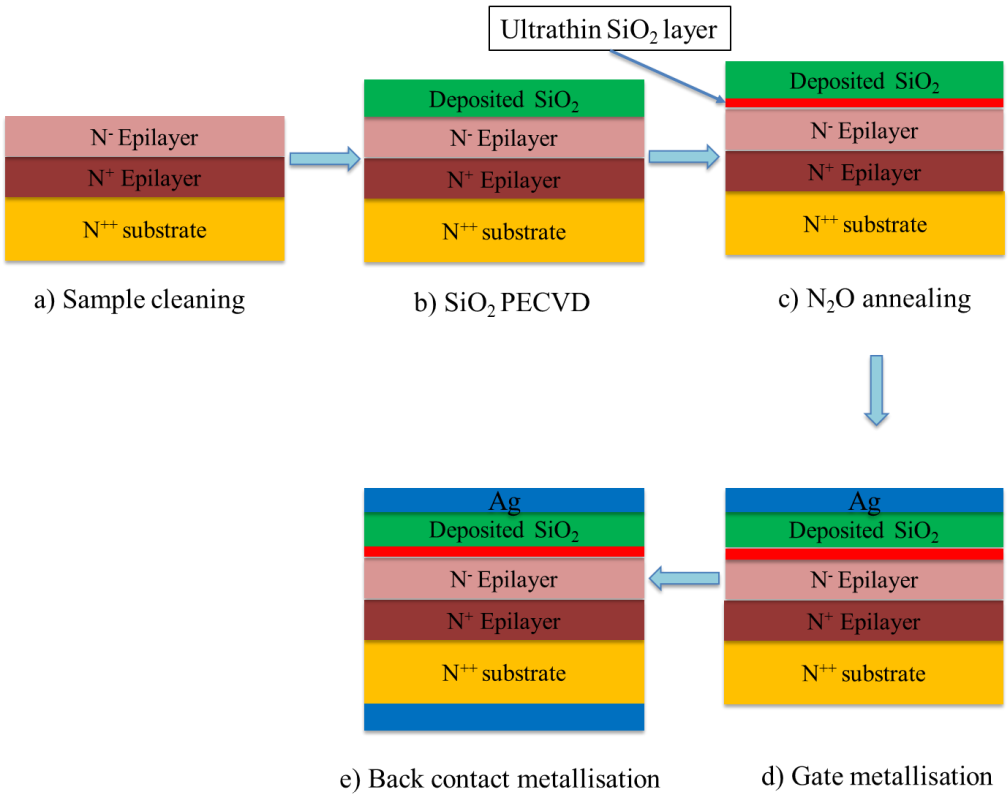


Figure 6.1: Steps of the n-type MOS capacitor fabrication process using deposited SiO_2.

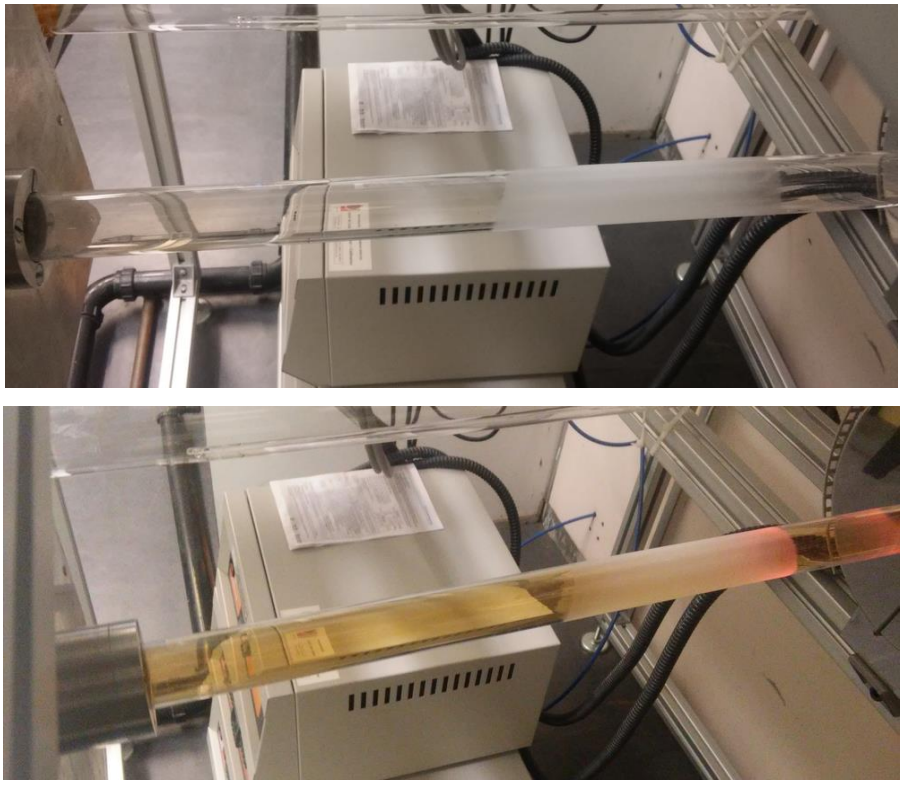


Figure 6.2: Change in colour in the furnace during POA in N_2O from colourless at room temperature (above) to brownish (below) after achieving a temperature of 700 °C.

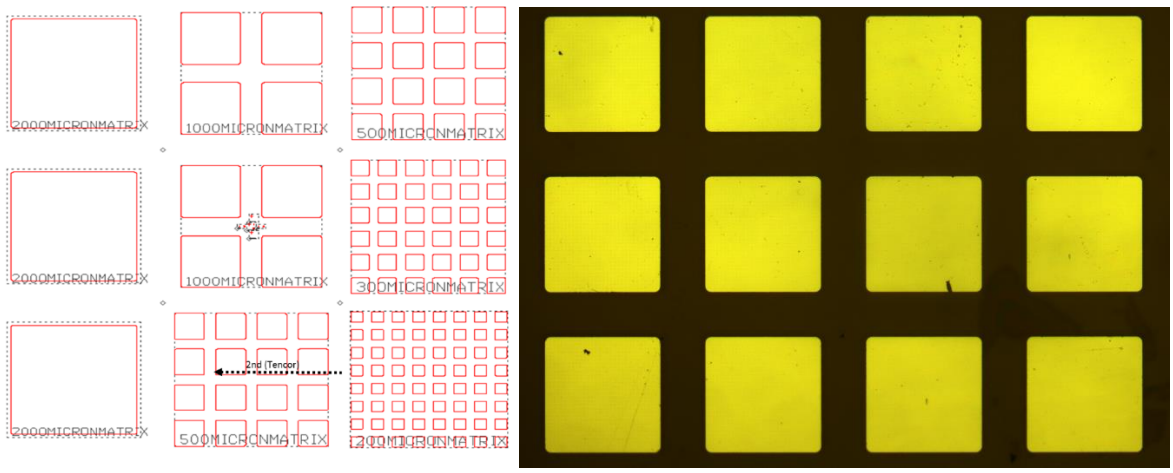


Figure 6.3: Mask set used to pattern (left) and fabricated n-type MOS capacitors (right).

6.3 Device Characterisation Results

The physical thickness of the deposited SiO_2 layer was determined using AFM. Details of the measurement technique have been explained in section 3.4.2. The grown ultrathin SiO_2 thickness after POA in N-rich ambient was estimated using the Deal-Grove model. Details of the Deal-Grove model have been explained in section 3.5.3. Accurate values of the physical thicknesses of both deposited and grown SiO_2 is important in order to correlate with the D_{it} values. Electrical characterisation, including I-V, C-V and G-V measurements, were performed on the fabricated MOS capacitors using the Agilent B1500A semiconductor device analyser. Temperatures up to 300 °C were applied to the samples through the chuck of the probe station for high temperature measurements.

6.3.1 Determination of deposited SiO_2 layer thickness

The SiO_2 was deposited on the 4H-SiC to form a gate oxide before being annealed in N-rich ambient. The non-contact AFM technique was used to determine the thickness of the deposited SiO_2. Figure 6.4 shows AFM images of deposited SiO_2 30 nm and 60 nm thick using PECVD. The verification of accurate SiO_2 thickness is important in order to estimate the thickness of the grown thin SiO_2 layer.

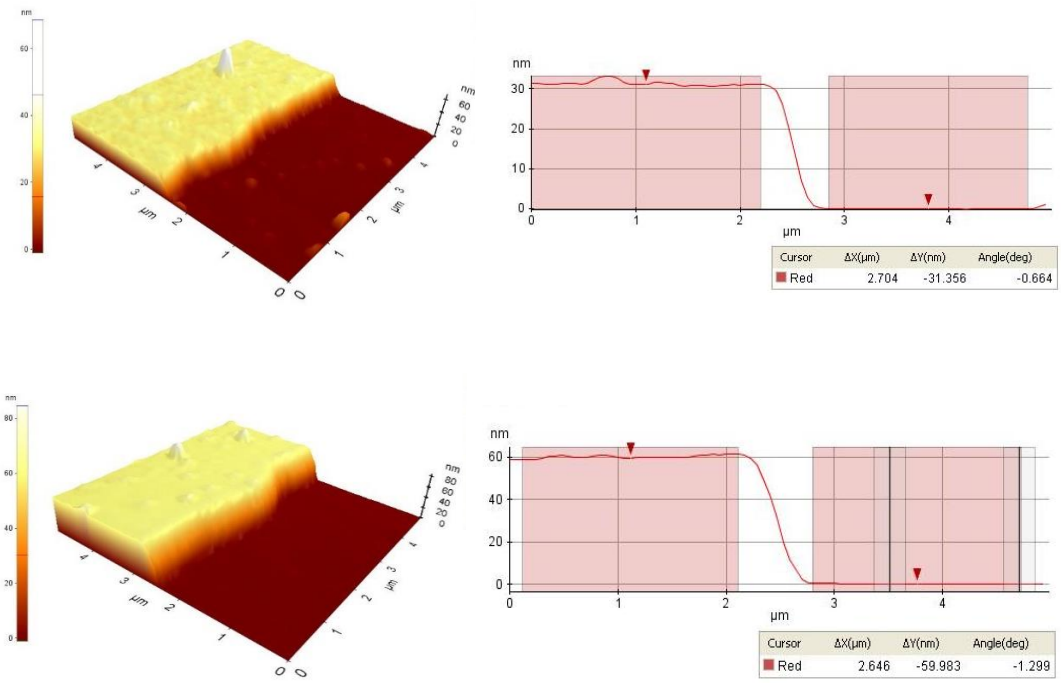


Figure 6.4: AFM images of (above) 30 nm and (below) 60 nm deposited SiO_2 using PECVD.

6.3.2 Determination of ultrathin SiO_2 layer thickness

After the deposition of SiO_2 at the gate, samples underwent an annealing process in N-rich ambient at 1175 °C to grow an ultrathin layer of SiO_2. The N_2O annealing process was used in order to achieve a lower growth rate which allows the growth of ultrathin layer thickness to be controlled compared to annealing in a pure O_2 ambient. The grown SiO_2 layer thickness underneath the deposited SiO_2 layer was estimated using the Deal-Grove model as given in equation 6.1 [104]:

$$\frac{dx}{dt} = \frac{B}{A+2x} \rightarrow Bt = Ax + x^2 \tag{6.1}$$

where the x is the grown SiO_2 thickness, t is the oxidation time and A and B are the parameters that need to be adjusted. Based on data from the initial oxidation in N_2O, the values of A and B are adjusted to be 11.84 and 1.00 respectively. Based on equation 6.1, the oxidation time in N_2O at 1175 °C is defined to be:

$$t = \frac{(L+x)^2 + A(L+x)}{B} - \frac{L^2 + A.L}{B} \tag{6.2}$$

where x is the grown SiO_2 thickness and L is the deposited SiO_2 thickness. Figure 6.5 shows the estimated grown SiO_2 thickness (x) as a function of oxidation time fitted using the Deal-

Grove model. The estimated grown SiO_2 using the Deal-Grove model is fitted to initial experimental data, proving that the estimation of thickness is acceptable.

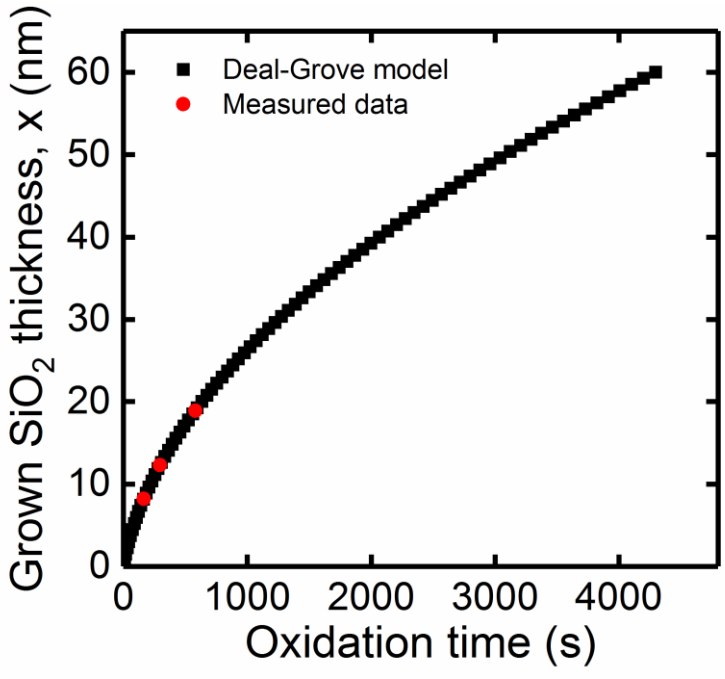


Figure 6.5: Estimated grown SiO_2 thickness (x) as a function of oxidation time in N_2O annealing ambient at 1175 °C fitted using the Deal-Grove model plotted with measured data for the Si-face (0001) 4H-SiC.

By using equation 6.2, the grown SiO_2 thicknesses are estimated for each of the oxidation times, with deposited SiO_2 thickness shown in Table 6.1.

Deposited SiO_2 thickness (nm)	**Oxidation time (min)**	**Estimated grown SiO_2 thickness (nm)**
30	30	0.42
30	60	0.84
30	120	1.68
60	30	0.23
60	60	0.46
60	90	0.68
60	120	0.91

Table 6.1: Estimated grown SiO_2 thickness based on the Deal-Grove model with different oxidation parameter.

6.3.3 Electrical characterisation of n-type MOS capacitor

In order to obtain a high quality of gate oxide, the number of traps should be reduced. Details of these traps have been discussed in section 3.2.2. Many researchers [46, 122] have suggested that interface trap charge is the main cause of poor channel mobility in MOSFETs. These traps are located at the oxide/4H-SiC interface and are measured in terms of their density (D_{it}). Values of D_{it} are measured by the electrical characterisation of MOS capacitors. In this chapter, the high-low method was used where a high frequency of 1 MHz and quasi-static (low) C-V were applied [80, 84]. Details of this measurement have been discussed in section 3.3.3. These measurements were then corrected for series resistance.

Figure 6.6(a) shows the distribution of D_{it} near the conduction band edge for n-type MOS capacitors extracted using the high-low method with a gate oxide consisting of deposited SiO_2 having a thickness of 30 nm. All devices were annealed in N_2O ambient at 1175 °C for 30, 60 and 120 min. From the results for all of these devices, the values of D_{it} maximum at 0.2 eV below conduction band edge and then decrease gradually with increasing energy. This D_{it} distribution near to the conduction band edge is similar to previous reports [7, 113, 159]. The device which was annealed for 60 min in N_2O ambient demonstrated the lowest D_{it} value of 2.26×10^{12} $cm^{-2}.eV^{-1}$ at an energy level of 0.2 eV near to the conduction band edge. From the estimation of thickness, this device has grown an SiO_2 ultrathin layer approximately 0.83 nm thick underneath the deposited SiO_2. Then the D_{it} at the 0.2 eV energy level near to the conduction band edge shows a slight increase to 2.63×10^{12} $cm^{-2}.eV^{-1}$ for the device that was annealed for 30 min. The highest D_{it} value of 4.87×10^{12} $cm^{-2}.eV^{-1}$ at an energy level of 0.2 eV near the conduction band edge was found with the device annealed for 120 min in N_2O ambient. The devices annealed for 30 min and 120 min produced ultrathin SiO_2 layers 0.42 nm and 1.64 nm thick respectively.

The correlation between the D_{it} values at an energy level of 0.2 eV near to the conduction band edge with an estimated thickness of the grown ultrathin SiO_2 layer is depicted in Figure 6.6(b). Each point of D_{it} plotted is the average from 5 different devices. From this plot, the lowest D_{it} value was obtained with a grown SiO_2 thickness of 0.83 nm in the device that was annealed for 60 min. This suggests that, at these annealing parameters, the grown SiO_2 has generated a lower concentration of C defects [33, 110]. However, as the annealing time increases, more traps are generated and thus the D_{it} value increases. On the other hand, as the annealing time is reduced down to 30 min, resulting in a grown SiO_2 layer 0.42 nm

thick, D_{it} values also increased. This may be caused by incomplete formation of the grown SiO_2 layer which does not result in a usable thickness [79, 124].

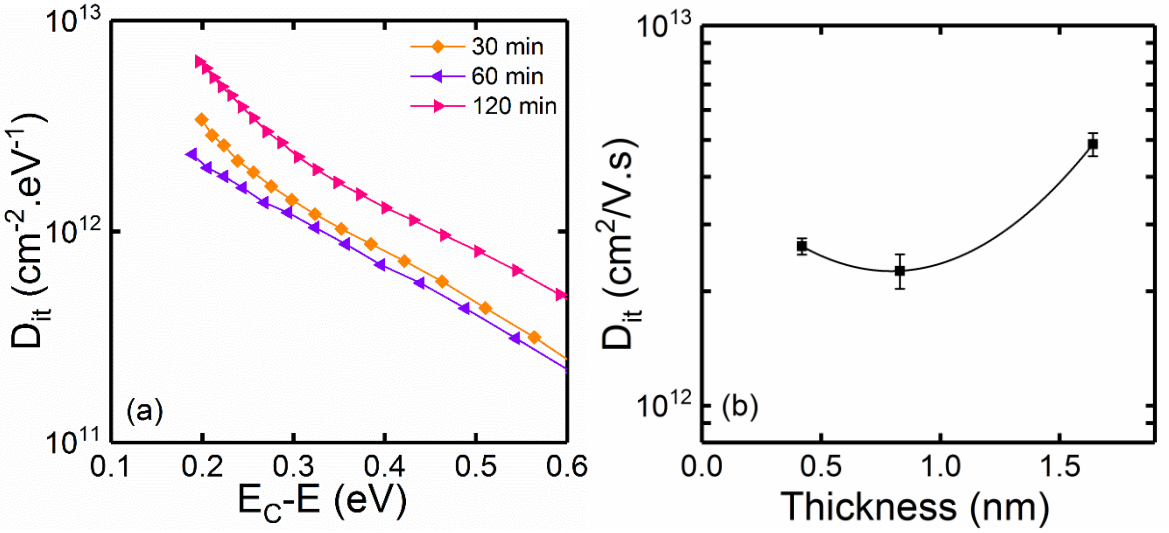


Figure 6.6: N-type MOS capacitors fabricated with 30 nm of deposited SiO_2 with different N_2O annealing times at 1175 °C (a) D_{it} distribution near conduction band edge and (b) D_{it} value at 0.2 eV energy level near conduction band edge as a function of grown oxide thickness.

To further optimise the annealing parameters in order to obtain the lowest values of D_{it}, MOS capacitors were also fabricated with a gate oxide consisting of a 60 nm thick deposited SiO_2 layer. This will allow the investigation of a wide range of annealing conditions. The annealing was performed with similar conditions with 30 nm of SiO_2 devices (N_2O at 1175 °C) to give a direct comparison. Figure 6.7(a) shows the D_{it} distribution extracted using the high-low method as a function of energy level near to the conduction band edge for fabricated n-type MOS capacitors. These devices have a gate oxide of 60 nm of deposited SiO_2, which is then annealed in N_2O ambient at 1175 °C for 30, 60, 90 and 120 min. A similar trend was observed for all the fabricated devices, where the D_{it} values decreased with increasing energy level in agreement with previous reports [7, 113, 159]. From these results for D_{it}, the device which was annealed for 90 min at 1175 °C showed the lowest values of D_{it}. D_{it} values as low as 1.76×10^{12} $cm^{-2}.eV^{-1}$ were obtained at the 0.2 eV below the conduction band edge. The devices which were annealed for 60 and 120 min produced almost similar values of D_{it} in the range of $2\text{-}3 \times 10^{12}$ $cm^{-2}.eV^{-1}$ at 0.2 eV below the conduction band edge. The highest D_{it} value of 5.41×10^{12} $cm^{-2}.eV^{-1}$ at the 0.2 eV below the conduction band edge was found for the devices that underwent an annealing for 30 min. This represents an increase in D_{it} of almost 5×10^{12} $cm^{-2}.eV^{-1}$ compared with the devices that experienced 90 min of annealing. The

thickness of grown SiO_2 underneath the 60 nm deposited SiO_2 corresponding to the N_2O annealing process for the fabricated devices is estimated using the Deal-Grove model [104].

Figure 6.7(b) shows the relationship of D_{it} values at 0.2 eV below the conduction band edge as a function of estimated grown oxide thickness. Each point of the D_{it} value is the average from 5 different devices. The lowest D_{it} value was obtained with devices annealed for 90 min and has grown a 0.68 nm thick layer of ultrathin SiO_2. As the annealing time increased up to 120 min, the D_{it} values also increased due to the formation of more C defects generated with higher temperature [33, 110]. Conversely, the D_{it} values decreased as the annealing temperature was reduced down to 60 and 30 min. This shows that a similar trend occurred with the 30 nm of deposited SiO_2 gate oxide where the value of D_{it} increased as the grown SiO_2 was less than 0.7 nm thick. This could also be explained by the incomplete formation of usable SiO_2 [79, 124].

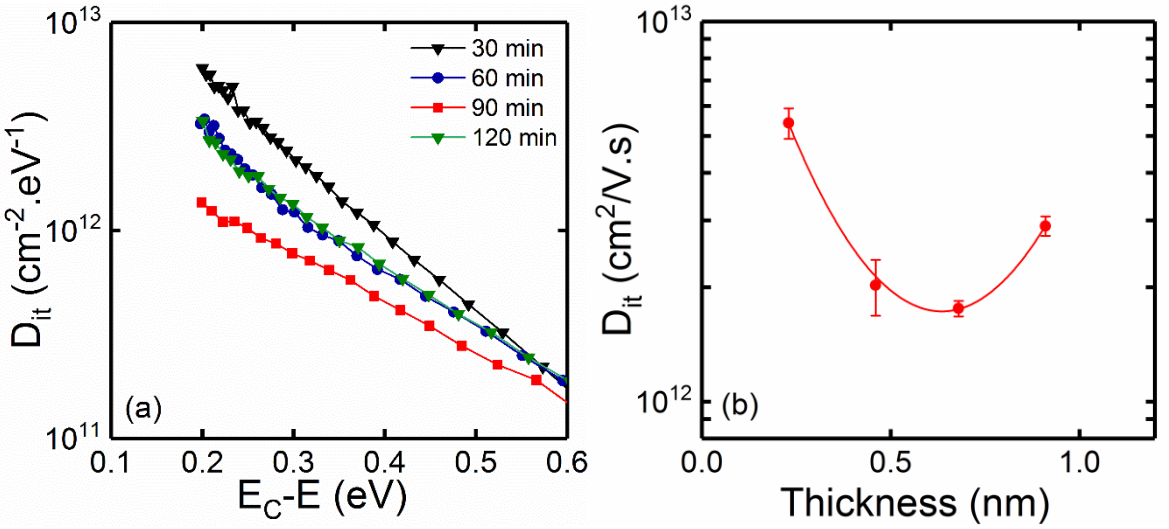


Figure 6.7: N-type MOS capacitors fabricated with 60 nm of deposited SiO_2 with different N_2O annealing times at 1175 °C (a) D_{it} distribution near conduction band edge and (b) D_{it} value at 0.2 eV energy level near conduction band edge as a function of grown oxide thickness.

Figure 6.8 shows a correlation between the D_{it} and the thickness of grown ultrathin SiO_2 for all the fabricated n-type MOS capacitors with 30 and 60 nm of deposited SiO_2. The D_{it} values as a function of grown SiO_2 thickness show a trend resembling a "valley", reaching the lowest values of D_{it} for a layer of grown SiO_2 0.68 nm thick. This is attributed to the generation of a lower C defects concentration which would degrade the interface quality. As the grown SiO_2 thickness increases, corresponding to a longer annealing time, higher C defects

concentrations were generated and hence the D_{it} values increased [33, 110]. On the other hand, the values of D_{it} also increased as the grown SiO_2 thickness became thinner. This suggests that the grown ultrathin SiO_2 layers with thicknesses less than 0.7 nm were not fully formed. To form a complete layer of SiO_2, modelling studies [79, 124] have suggested that it needs to be at least 4 silicon (Si) atoms across, which corresponds to SiO_2 approximately 0.7 nm thick. These first principles studies support the present findings, confirming that 0.68 nm thick SiO_2 is the thinnest complete and usable SiO_2 layer. A similar trend was also observed in chapter 4, where the lowest obtained D_{it} values were shown by the MOS capacitors with gate oxide grown to an approximate thickness of 0.7 nm of SiO_2.

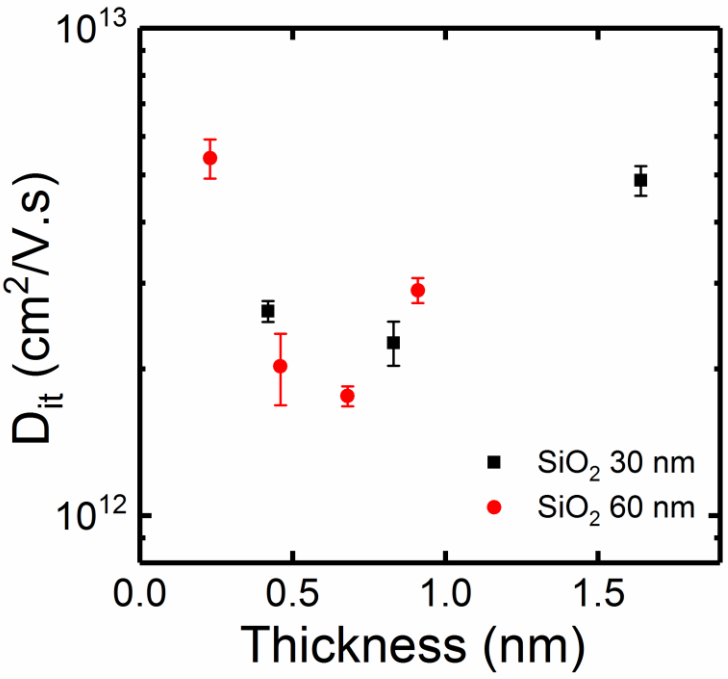


Figure 6.8: D_{it} values at energy level of 0.2 eV as a function of grown ultrathin SiO_2 thickness for gate oxide with 30 and 60 nm of deposited SiO_2 in n-type MOS capacitors.

In addition to the study of D_{it}, values of effective oxide charge density (N_{eff}) were also determined for all of the fabricated devices to access the oxide quality. Details of the extraction and definition of N_{eff} are discussed in section 3.2.2. N_{eff} consists of fixed charge (Q_f), oxide trapped charge (Q_{ot}) and mobile charge (Q_m) which are generated by the method during the oxide formation process. Figure 6.9 shows a correlation between values of D_{it} at the energy level of 0.2 eV with the values of N_{eff} for all of the fabricated n-type MOS capacitors. Each point of the D_{it} and N_{eff} values is the average from 5 different devices. MOS capacitors having a deposited SiO_2 gate oxide 60 nm thick followed by annealing at 1175 °C for 90 min show the lowest values in D_{it} as well as low values of N_{eff}. N_{eff} values as low as -3.46×10^9 cm^{-2}

were found in such devices. This further demonstrates that such a thickness of deposited SiO_2 and these N_2O annealing conditions are the best to produce the gate oxide with highest quality. As D_{it} increases, the values of N_{eff} for most of the devices increased, showing that D_{it} is directly proportional to N_{eff} as shown in Figure 6.9. This suggests that all of the trap types can be reduced by a similar gate oxide formation technique.

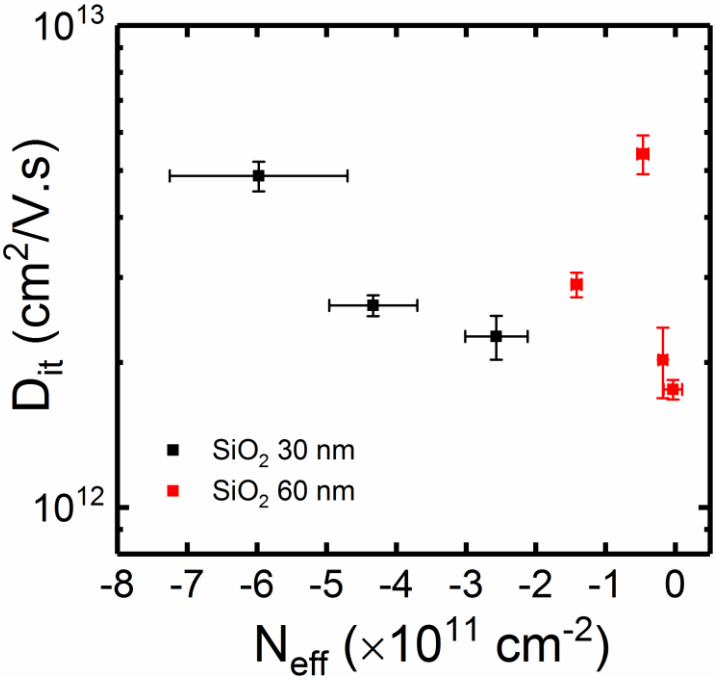


Figure 6.9: D_{it} values at energy level of 0.2 eV as a function of effective oxide charge density for all fabricated n-type MOS capacitors.

In addition, MOS capacitors were also fabricated with a gate oxide that had an annealed in nitrogen (N_2) ambient, in order to further study the effect of N_2 on the deposited SiO_2 gate oxide. Devices were deposited with 30 and 60 nm thick SiO_2 before undergoing annealing in N_2 at 1175 °C for 120 min. This annealing process will not produce an ultrathin layer of SiO_2 underneath the deposited SiO_2 due to the fact that N_2 gas does not contain the oxygen (O) atoms which are required to grow the SiO_2. But these N atoms are believed to be able to penetrate underneath the deposited SiO_2 and passivate the dangling bonds of the 4H-SiC and thus improve interface quality [42, 43]. However, neither of these devices could be characterised due to high leakage at the gate oxide. Similar behaviour can also be found with the devices that did not experience any annealing process for both 30 and 60 nm of deposited SiO_2. These high leakage currents occurred due to the fact that the quality of the oxide/4H-SiC interface for such devices is poor. The bonding between 4H-SiC and the oxide is not formed properly, leaving a large number of dangling bonds. During growth of an ultrathin

SiO_2 layer, strong bonds are formed between SiO_2 and 4H-SiC. An excess of dangling bonds are believed to be passivated by nitrogen (N) atoms during the N_2O annealing process. Table 6.2 shows details of the gate oxide formation conditions with extracted values in order to determine the quality of fabricated n-type MOS capacitors. The theoretical values of flatband voltage (V_{fb}) of all the fabricated devices is calculated to be 0.5 V. The shift in V_{fb} is mainly due to the presence of N_{eff} in the oxide [80, 84]. Details of the V_{fb} value calculation have been discussed in section 3.3.1.

Deposited SiO_2 (nm)	**POA in N_2O at 1175 °C (min)**	**POA in N_2 at 1175 °C (min)**	**Estimated SiO_2 Thickness (nm)**	**V_{fb} (V) ($V_{fb\ (theory)}$ = 0.5 V)**	**N_{eff} (cm^{-2})**	**D_{it} ($cm^{-2}.eV^{-1}$)**
30	-	-	-	Leakage		
30	-	120	-	Leakage		
30	30	-	0.42	1.27	-4.33×10^{11}	2.63×10^{12}
30	60	-	0.83	0.98	-2.57×10^{11}	2.26×10^{12}
30	120	-	1.64	1.63	-5.98×10^{11}	4.87×10^{12}
60	-	-	-	Leakage		
60	-	120	-	Leakage		
60	30	-	0.23	0.63	-4.66×10^{10}	5.41×10^{12}
60	60	-	0.46	0.57	-1.80×10^{10}	2.02×10^{12}
60	90	-	0.68	0.52	-3.46×10^{9}	1.76×10^{12}
60	120	-	0.91	1.00	-1.42×10^{11}	2.90×10^{12}

Table 6.2: Details of gate oxide formation parameter with extracted values for all fabricated n-type MOS capacitors

6.3.4 High temperature measurement

Among the objectives for the fabrication of 4H-SiC MOS devices is for them to be operational in high temperature environments. In this section, n-type MOS capacitors with the gate dielectric consisting of (i) 30 nm deposited SiO_2 followed by 60 min of N_2O annealing at 1175 °C and (ii) 60 nm deposited SiO_2 followed by 90 min of the N_2O annealing at 1175 °C were investigated to examine the device performance over a wide range of temperatures. Both devices exhibited the lowest values of D_{it} at room temperature for each of the deposited SiO_2

thicknesses of 30 and 60 nm, as described in section 5.4.3. Figure 6.10 shows the C-V characteristics for the forward sweep of n-type MOS capacitors for temperatures up to 300 °C. Both of the devices demonstrate a positive shift, as the measured temperature increases up to 300 °C. This trend is studied along with the change in V_{fb} against elevated temperature. Details of the V_{fb} calculation have been explained in section 3.3.1.

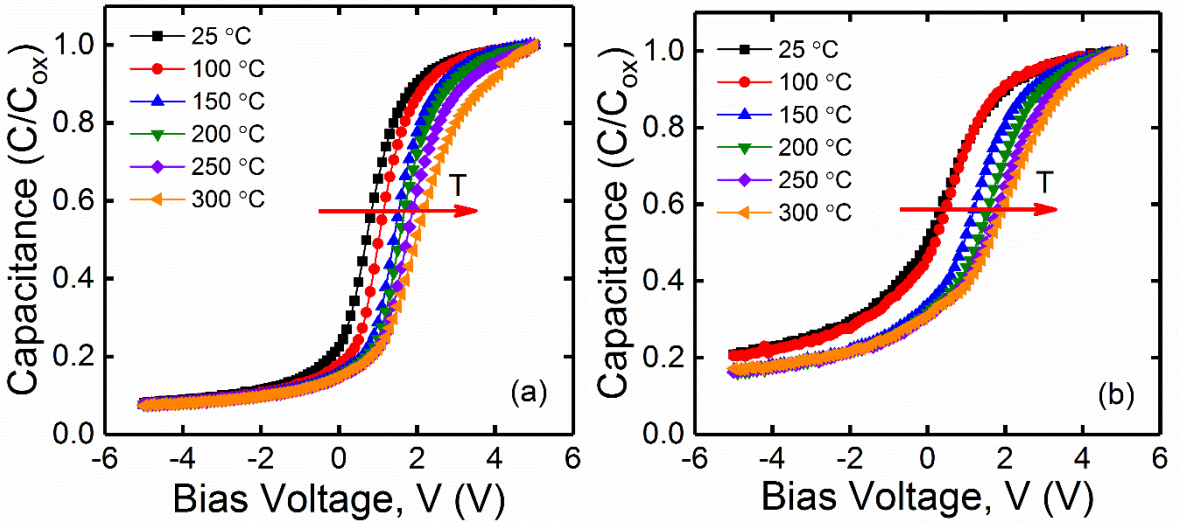


Figure 6.10: C-V characteristics for fabricated n-type MOS capacitor with gate oxide consisting of (a) deposited SiO_2 60 nm thick followed by N_2O annealing for 90 min and (b) deposited SiO_2 30 nm thick followed by N_2O annealing for 60 min, plotted against temperature.

Figure 6.11 shows the V_{fb} value measured at 1 MHz for the forward and reverse sweeps for both devices. Each point of the V_{fb} value is the average from 5 different devices. The V_{fb} at room temperature during the forward sweep for the deposited SiO_2 30 and 60 nm thick were 0.98 V and 0.52 V respectively. As the measured temperature increases, the V_{fb} gradually increased up to 2.3 V and 2.1 V at 300 °C for 30 and 60 nm thick deposited SiO_2 devices respectively. A similar trend was also found during the reverse sweep of the C-V characteristics. The extracted V_{fb} at room temperature for 30 and 60 nm thick deposited SiO_2 were 1.36 V and 0.82 V before increasing up to 2.90 V and 3.32 V at 300 °C respectively. Overall, both devices demonstrated an increase in V_{fb} of approximately 2-3 V from room temperature up to 300 °C for both forward and reverse sweeps. This may be correlated with the effect of electron injection during accumulation bias [90, 160-162].

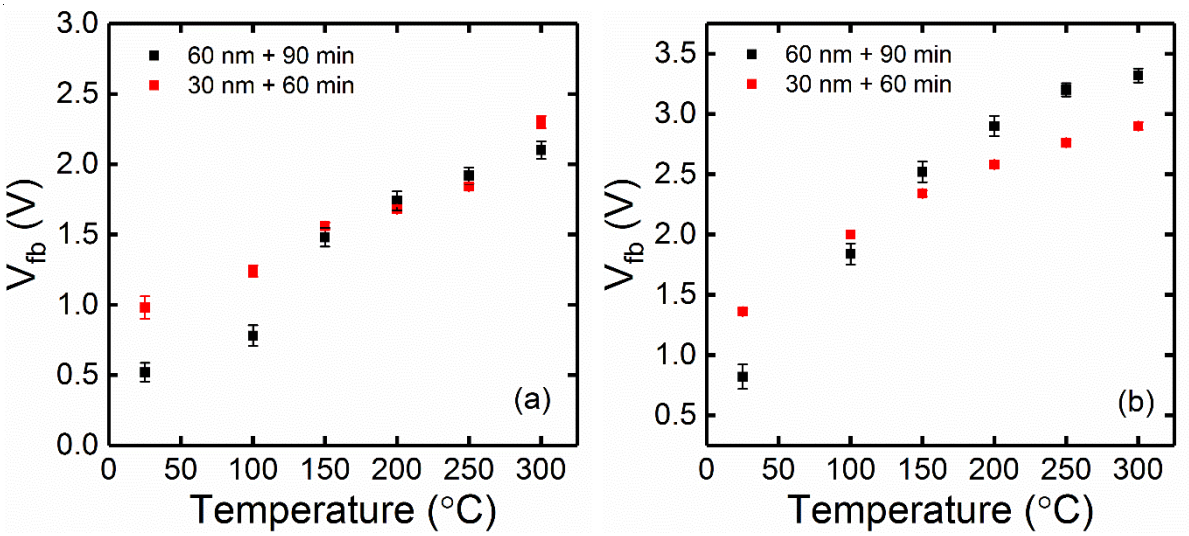


Figure 6.11: V_{fb} measured at 1 MHz versus temperature for (a) forward sweep and (b) reverse sweep from C-V measurements for n-type MOS capacitors

The change in V_{fb} against the measured temperature can also be determined at different measurement frequencies in order to study the stability of the devices. Figure 6.12 shows the bidirectional characteristic of the V_{fb} values for both devices at different frequencies. Each point of the V_{fb} value is the average from 5 different devices. The data for the forward sweep measurements for both devices show almost similar values of V_{fb} at 10 kHz and 100 kHz, but these are reduced slightly as the measurement frequency is increased up to 1 MHz for most of the temperatures measured. For the reverse sweep measurements, the results show an increase in V_{fb} at a frequency of 1 MHz for the 60 nm deposited SiO_2 devices. Contrarily, the V_{fb} were almost unchanged regardless of measurement frequencies during the reverse sweep measurements of the 30 nm deposited SiO_2 devices. Overall, both devices demonstrate minor variations in V_{fb} with frequency for elevated temperatures. This could suggests that both devices were stable against measurement frequencies and this may be attributed to the high quality of the gate oxide formed [163].

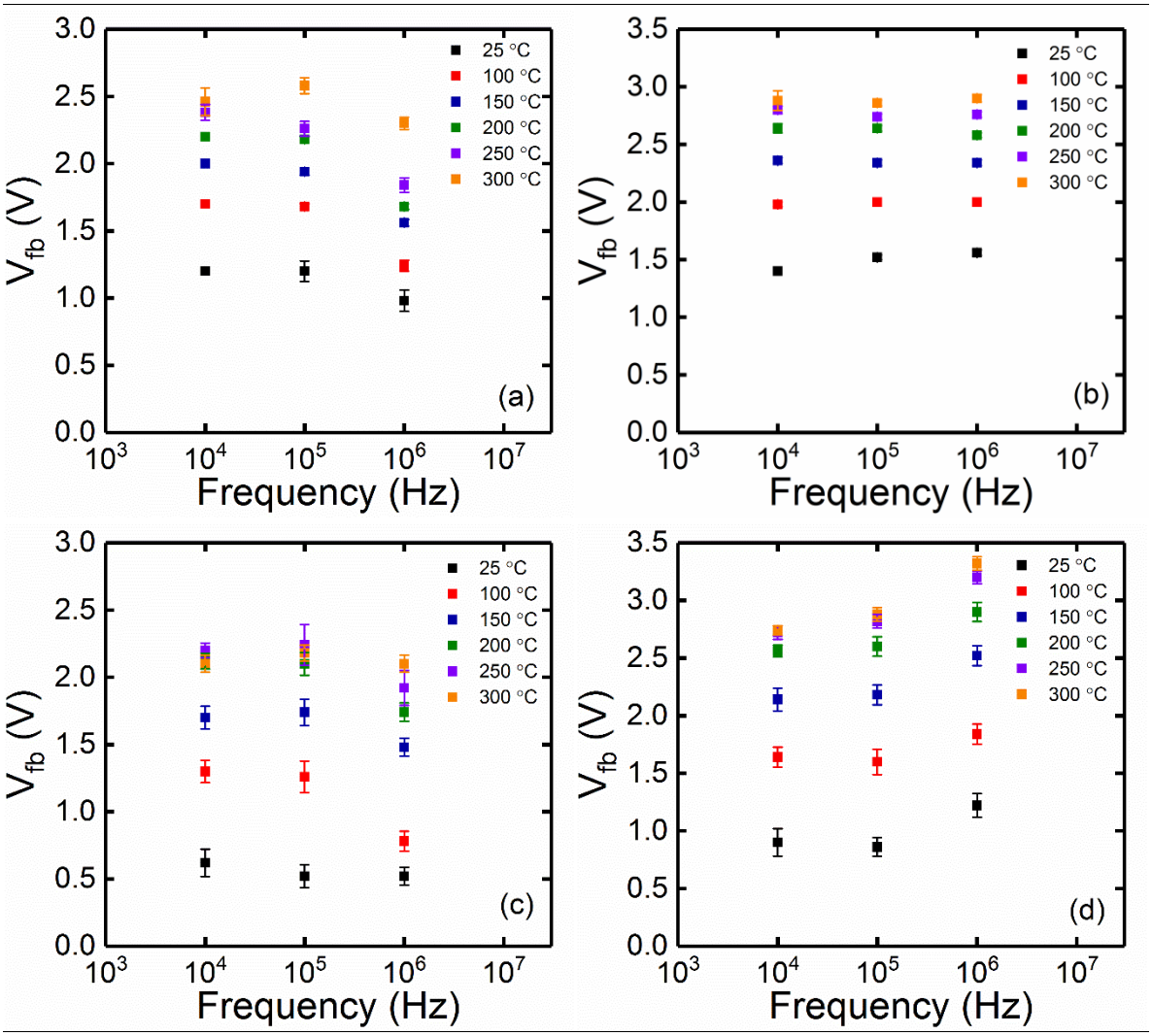


Figure 6.12: V_{fb} during (a) forward sweep and (b) reverse sweep for 30 nm deposited SiO2 devices and (c) forward sweep and (d) reverse sweep for 60 nm deposited SiO2 devices extracted from C-V measurements plotted as a function of measurement frequency.

The concentration of trap charges in the oxide which degrade device stability can be calculated based on the ideal C-V curve. Figure 6.13 shows the values of N_{eff} measured at 1 MHz for forward and reverse sweeps for both devices as a function of measured temperature. Each point of the N_{eff} value is the average from 5 different devices. The N_{eff} values of the forward sweep for 60 nm deposited SiO_2 devices are as low as -3.46×10^9 cm^{-2} at room temperature and gradually increase with temperature, peaking with N_{eff} values of -3.74×10^{11} cm^{-2} at 300 °C. This represents an increase in N_{eff} by 2 orders of magnitude as the temperature increases from room temperature to 300 °C. The same increase with temperature in N_{eff} values was found during the forward sweep for the 30 nm thick deposited SiO_2 devices, which were -2.57×10^{11} cm^{-2} at room temperature and then increased to as high as -9.10×10^{11} cm^{-2} at 300 °C. For the reverse sweep measurements, both devices showed an increase in N_{eff} of around

5.0×10^{11} cm^{-2} with increasing temperature. In general, both devices demonstrate an increase in N_{eff} values with temperature regardless of sweep direction. This trend may be due to changes in the concentration of charges in the oxide as temperature increases [163].

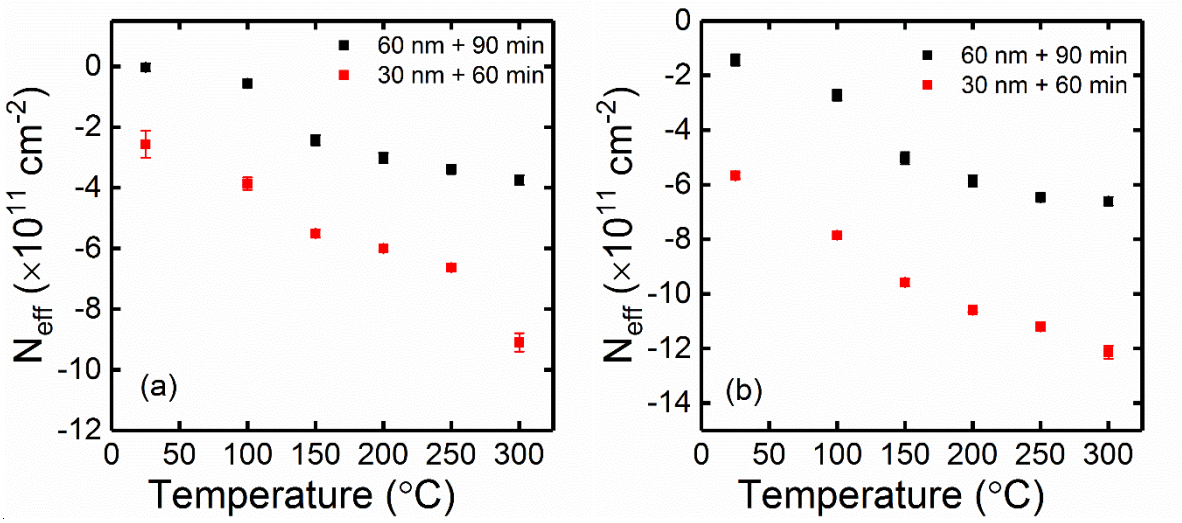


Figure 6.13: Effective oxide charge N_{eff}, for n-type MOS capacitors as a function of measured temperature measured at 1 MHz for the (a) forward sweep and (b) reverse sweep.

Figure 6.14 shows the hysteresis of V_{fb} measured at 1 MHz for both 30 and 60 nm deposited SiO_2 devices as a function of elevated temperature. The hysteresis voltage value was calculated from the differences in V_{fb} between the forward and reverse sweeps. Each point of the ΔV_{fb} value is the average from 5 different devices. For devices having a 30 nm deposited SiO_2 gate oxide, ΔV_{fb} was relatively consistent with values less than 1 V for the whole range of measured temperatures. However, a rise in ΔV_{fb} was observed for the 60 nm deposited SiO_2 devices with temperature. At room temperature, the ΔV_{fb} was found to be 0.3 V before surging with increasing temperature. A peak value of 1.3 V was obtained at 250 °C before a slight decrease by 0.1 V as the measured temperature reached 300 °C. The origin of this variation could be explained by the effect of the trapping and de-trapping of electrons in the bulk SiO_2 [161, 164].

Moreover, the D_{it} values were also extracted against a range of temperatures in order to observe the interface trap charges behaviour at high temperature. Figure 6.15 shows the D_{it} values at 0.2 eV below the conduction band edge extracted using the high-low method for both devices as a function of measured elevated temperature. Each point of the D_{it} value is the average from 5 different devices. D_{it} values of approximately 2.26×10^{12} $cm^{-2}.eV^{-1}$ and $1.76 \times$

10^{12} $cm^{-2}.eV^{-1}$ were obtained at room temperature, then decreasing down to 6.61 × 10^{11} $cm^{-2}.eV^{-1}$ and 5.94 × 10^{11} $cm^{-2}.eV^{-1}$ at 300 °C for 30 and 60 nm deposited SiO_2 respectively. The reduction of D_{it} with increasing temperature for both devices is due to the excitation of interface trap charges at higher temperature. Moreover, the bandgap narrowing effect which occurs at higher temperatures has moved the conduction band closer to the valence band and hence the value of D_{it} at the band edges is reduced [127]. The reduction of bandgap with temperature is shown in Figure 3.3. D_{it} also decreases with temperature in the Si-SiO_2 system [128].

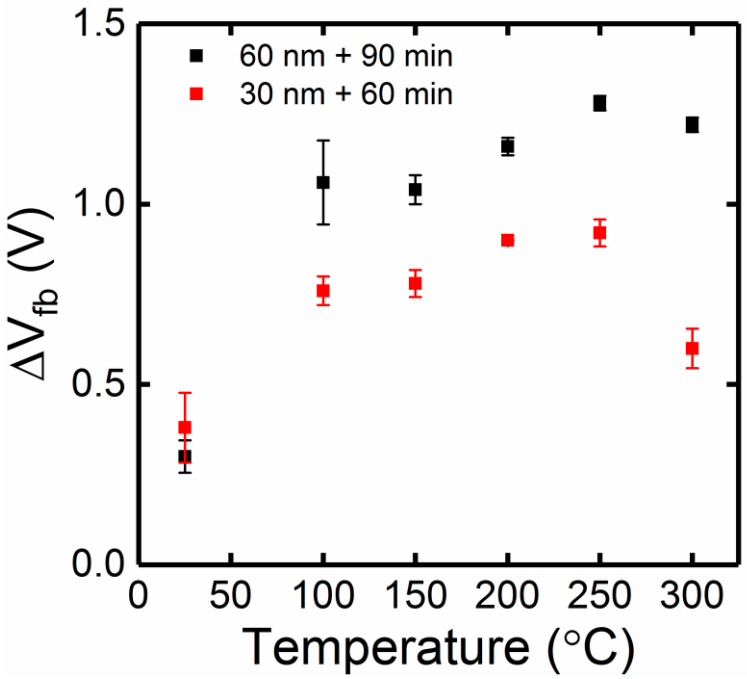


Figure 6.14: Change in flatband voltage ΔV_{fb} extracted at 1 MHz for fabricated n-type MOS capacitors as a function of temperature.

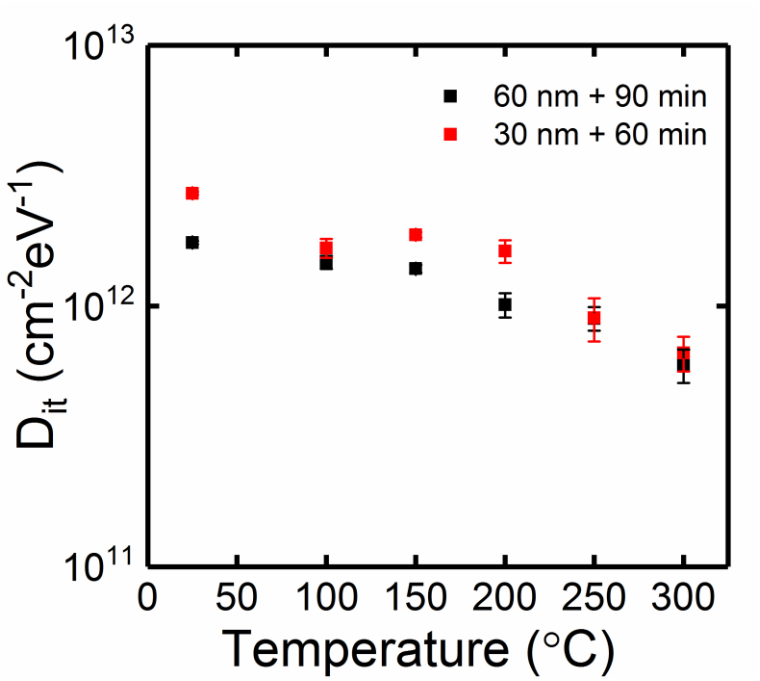


Figure 6.15: Values of D_{it} at the 0.2 eV energy level near to the conduction band edge extracted using the high-low method versus temperature.

6.3.5 Current Conduction Mechanism

The current conduction mechanism of the fabricated MOS capacitors was determined using I-V characterisation. In this section, MOS capacitors with 60 nm of deposited SiO_2 followed by 90 min N_2O annealing at 1175 °C were investigated. Figure 6.16 shows the leakage current density as a function of electric field in the oxide of the 60 nm deposited SiO_2 device. The gate oxide started to experience electron injection at 6 MV/cm at leakage current densities as low as 1×10^{-9} A/cm^2 before breakdown at 9.4 MV/cm. This value is in agreement with those of previous reports [129, 157, 158], where a breakdown field of around 10 MV/cm was found for SiO_2 deposited on 4H-SiC. In comparison, the dielectric breakdown for thermally grown SiO_2 on Si also showed a similar value of 10 MV/cm [165]. This suggests that the gate oxide with 60 nm deposited SiO_2 followed by 90 min N_2O annealing is robust and suitable for operation in high electric fields.

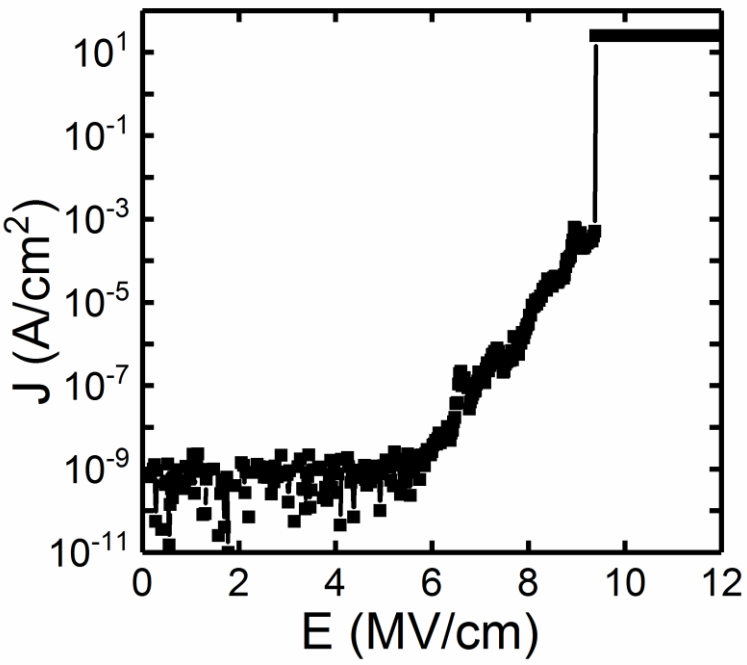


Figure 6.16: Current density as a function of the oxide electric field of fabricated n-type MOS capacitor with 60 nm thick deposited SiO_2 followed by N_2O annealing for 90 min at 1175 °C.

To further investigate the leakage current conduction mechanism, Fowler-Nordheim (F-N) injection was studied. Figure 6.17 depicts the F-N plot at a high oxide field above 8 MV/cm for the MOS capacitor fabricated with a gate oxide formed with 60 nm deposited SiO_2 followed by N_2O annealing. The excellent linear relationship over three orders of magnitude of current suggests that F-N electron tunnelling governs current conduction [12, 131, 136, 166]. The inset figure shows the extended F-N plot of the device. By fitting the F-N plot to equation 4.9, the barrier height ϕ_B, of the deposited oxide relative to 4H-SiC can be obtained. From the fitting results using $m_{ox} = 0.42m_o$ [130, 166], a value of $\phi_B = 2.55$ eV was found for the 60 nm deposited SiO_2 followed by the N_2O annealing of gate oxide. This value is less than that reported by Kimoto *et al*. [158] with ϕ_B was 2.84 eV, where the gate oxides were formed by deposited SiO_2 followed by N_2O annealing. Furthermore, for dry oxidation SiO_2 gate oxides that have experienced N_2O annealing, the reported ϕ_B values vary from 2.58 to 2.74 eV [130, 167, 168] indicates that the ϕ_B value of our fabricated devices are slightly less but in agreement with other gate oxides. However, based on theoretical calculations [168, 169], the value of ϕ_B for F-N tunnelling current is 2.7 eV for the SiO_2/4H-SiC system, which is slightly higher than that found in our fabricated devices.

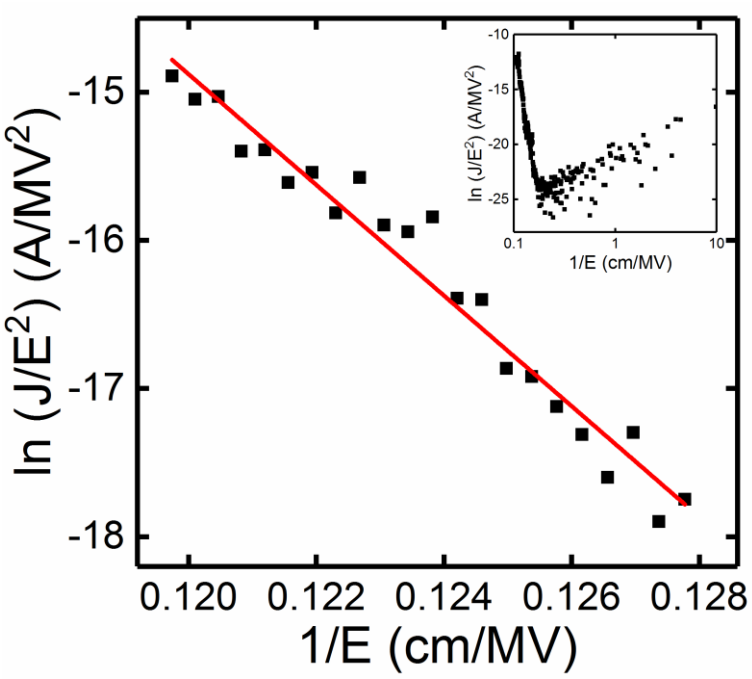


Figure 6.17: Fowler–Nordheim plot (inset: extended Fowler–Nordheim plot), for fabricated n-type MOS capacitors with 60 nm thick deposited SiO_2 followed by N_2O annealing for 90 min at 1175 °C.

6.4 Key Findings and Conclusion

In this chapter, 4H-SiC MOS capacitors were successfully fabricated with a vertical geometry on n-type epitaxial material. The gate oxides, which are the key factor, were formed by the deposition of SiO_2 using PECVD followed by N-rich annealing at 1175 °C. The POA in N_2O was used to grow an ultrathin layer of SiO_2 underneath the deposited SiO_2 to passivate the dangling bonds of the 4H-SiC. The grown SiO_2 thickness was estimated using the Deal-Grove model based on initial experimental data.

The lowest value of D_{it} for the fabricated MOS capacitors was formed using a gate oxide of 60 nm deposited SiO_2 followed by N_2O annealing for 90 min at 1175 °C. This produced 0.68 nm SiO_2 underneath the deposited SiO_2 layer. By using the high-low method, D_{it} values as low as 1.76×10^{12} $cm^{-2}.eV^{-1}$ were measured at 0.2 eV below the conduction band edge. Furthermore, the devices also produced the lowest values of N_{eff} of approximately -3.46 $\times 10^9$ cm^{-2}. The values of D_{it} from all of the devices show a correlation with the thickness of the grown ultrathin SiO_2 layer. The D_{it} values of the fabricated devices increased as the grown SiO_2 thickness increased above 0.68 nm. This supports the notion that larger concentrations of C defects were generated from the SiC substrate over time at high temperature. The high

concentration of C defects increased the values of D_{it} and hence the quality of the oxide/4H-SiC interface deteriorated. On the other hand, the D_{it} values also reduced as the grown SiO_2 thickness decreased to less than 0.68 nm. This suggests that the grown SiO_2 layer was not fully or uniformly formed, since the thinnest usable SiO_2 layer was estimated to be around 0.7 nm.

Electrical measurements up to 300 °C proved that the devices are able to operate properly at high temperature. The V_{fb} shows a positive shift as the measured temperature increased for both of the devices studied. This is mainly due to the electron injection during accumulation. ΔV_{fb} values less than 0.5 V were obtained for both devices studied at room temperature, which are smaller than that found using the Al_2O_3 gate stack as discussed in chapter 4. However, a variation in voltage hysteresis was observed with elevated temperature, indicating that trapping and de-trapping effects occurred in the gate oxide during the bidirectional C-V measurements. A reduction in values of D_{it} with increasing temperature was also noticed, indicating the occurrence of electron excitation from the traps as well as a bandgap narrowing effect.

The devices with 60 nm deposited SiO_2 followed by 90 min N_2O annealing also showed an excellent leakage current mechanism. Based on F-N plots, the devices produced a value of ϕ_B of 2.55 eV, which is deemed to be sufficient and it could also withstand oxide electric fields as high as 9.4 MV/cm with a leakage current density of approximately 1×10^{-3} A/cm^2. This study of the current conduction mechanism has thus proven that the fabricated gate oxide is robust.

In conclusion, 60 nm thick deposited SiO_2 using PECVD followed by 90 min N_2O annealing represent the best parameters to form a gate oxide for the MOS capacitor. A 0.68 nm thick ultrathin layer of SiO_2 was grown and has generated low values of D_{it} as well as N_{eff}. The gate oxide formed is also stable at high temperature and robust, proving that these are the best parameters to use in fabricating a MOS capacitor.

Chapter 7

Summary and Conclusions

7.1

This research has focused on both fabrication and characterisation in developing a good dielectric/4H-SiC interface for MOS devices. This aim was realised by the introduction of an ultrathin SiO_2 layer between the deposited dielectric and 4H-SiC. In chapter 4 of this thesis, the MOS capacitors which are the key component of MOS devices have been fabricated for use in analysing the quality of the interface. The gate dielectric of the devices was formed by growing an ultrathin SiO_2 layer followed by the deposition of Al_2O_3 using Atomic Layer Deposition (ALD). The ultrathin SiO_2 layer was grown using a low thermal budget technique using Rapid Thermal Processing (RTP). The Angle Resolved X-Ray Photoelectron Spectroscopy (ARXPS) technique was used to estimate the grown SiO_2 layer thickness. A wide range of oxidation parameters were optimised in order to obtain a low value of density of interface traps (D_{it}), which are believed to be the main source of the degradation of interface quality. Carbon (C) defects are believed to be generated during thermal oxidation and then become the source of D_{it}. It is well recognised that D_{it} are electrically active (Coulomb scattering) and degrade electron mobility in MOSFETs. Therefore, a low thermal budget technique is introduced in order to minimise the generation of C defects. In this thesis, all D_{it} were extracted using a high-low C-V method that utilised 1 MHz for high and quasi-static mode for low frequency.

P-type MOS capacitors were fabricated by forming the gate dielectric before and after the formation of the metal-semiconductor (MS) contact. This step is important because the MS

contact needs to be annealed at 1000 °C for 3 min in order to reduce the specific contact resistance (ρ_c) and to thus demonstrate ohmic contact behaviour. From the electrical characterisation results, the gate stack consisting of an ultrathin SiO_2 layer grown at 600 °C for 3 min after post-metallisation annealing (PMA) showed the lowest D_{it} values of 4.2×10^{11} $cm^{-2}eV^{-1}$ at 0.2 eV above the valence band. This represents a reduction in D_{it} by one order of magnitude compared to gate stack formed before PMA using similar oxidation conditions (600 °C for 3 min). The grown SiO_2 layer was estimated to be 0.7 nm thick using ARXPS for such oxidation parameters. The PMA performed at high temperature before gate stack formation is believed to have increased the generation of C defects and thus the quality of the dielectric/4H-SiC interface deteriorated. This was further confirmed by the D_{it} results of the MOS capacitors fabricated with gate dielectric formed via oxidation at 1150 °C for 180 min in the furnace. High D_{it} values of approximately 2.0×10^{13} $cm^{-2}eV^{-1}$ at 0.2 eV above the valence band edge were obtained for such devices regardless of surface preparation. This represents an increase by two orders of magnitude compared with the devices consisting of the 0.7 nm (ultrathin) SiO_2 layer, which were grown after PMA. N-type MOS capacitors were also fabricated in a wide range of oxidation conditions in order to further verify the quality of the dielectric/4H-SiC interface using a low thermal budget technique. The lowest D_{it} values of 6.0×10^{11} $cm^{-2}eV^{-1}$ at 0.2 eV below the conduction band edge were obtained from the devices fabricated with SiO_2 grown at 600 °C for 3 min followed by Al_2O_3 deposition. This further verified the conclusion that such conditions are the best parameters to use in order to reduce the value of D_{it} and thus enhance the quality of the dielectric/4H-SiC interface. High temperature measurements up to 300 °C were performed, demonstrating that both p-type and n-type MOS capacitors with ultrathin SiO_2 layers grown at 600 °C for 3 min are durable and suitable for use in hostile environments. Furthermore, these devices exhibited an effective barrier height, ϕ_B of 1.35 eV, as calculated from the Fowler-Nordheim tunnelling plot, and were able to withstand an electric field of 6.5 MV/cm with a leakage current density of around 1×10^{-8} A/cm^2, thereby demonstrating that this gate dielectric is robust.

Having successfully obtained a low value of D_{it} for MOS capacitors, n-channel MOSFETs were fabricated using a similar technique. In Chapter 5 of this thesis, the fabrication and characterisation of the MOSFETs are discussed. In order to fabricate the n-channel MOSFET, the source and drain regions were formed by ion implantation of nitrogen (N). Then a carbon cap layer was formed on the 4H-SiC substrate in order to prevent the out-diffusion of

the implanted ions during the activation process. After that, the carbon cap was removed and typically this removal process was performed via oxidation at ~700-950 °C. However, in order to keep the thermal budget as low as possible, several removal techniques were performed in order to minimise the generation of C defects as well as to produce a minimum value of surface roughness, which is another main factor limiting electron mobility in MOSFETs. As a result, the carbon cap was effectively removed using a plasma asher for 90 min at room temperature, resulting in a low value of surface roughness of 0.46 nm.

High channel field effect mobility up to 125 cm^2/Vs at an effective electric field (E_{eff}) of 0.35 MV/cm with a subthreshold slope (SS) of 130 mV/dec were obtained from the MOSFETs fabricated with 0.7 nm SiO_2 grown at 600 °C for 3 min followed by Al_2O_3 deposition. Electron mobility remains as high as 94 cm^2/Vs at a higher E_{eff} of 0.6 MV/cm corresponding with E_{eff} in the gate dielectric of 3 MV/cm. This electron mobility is much higher than that in MOSFETs having a gate dielectric grown at 1150 °C for 180 min, where the peak mobility is only 7 cm^2/Vs. This represents a factor of 18× greater peak mobility using the gate dielectric grown at 600 °C for 3 min followed by Al_2O_3 deposition. A high current carrying capability was also observed in these devices and ratios up to 120 were demonstrated at a gate overdrive (V_{GS}-V_{th}) of 1.7 V over the gate dielectric grown at 1150 °C for 180 min. A well-recognised concern about the nature of Al_2O_3 is that it consists of 5 stable charge states in the bandgap, leading to large threshold voltage hysteresis (ΔV_{th}) between the forward and reverse sweeps of the I_D-V_{GS} curve. A densification process for the deposited Al_2O_3 was investigated in a range of low temperatures between 150-400 °C for 60 min. A reduction from 4 V for as-deposited Al_2O_3 film to 0.7 V following the densification process at 300 °C for 60 min was obtained. High temperature measurements up to 300 °C were performed on MOSFETs with both high and low electron mobility. For MOSFETs having gate dielectrics grown at 600 °C for 3 min, the electron mobility was reduced with increasing temperature, showing that mobility is limited by phonon scattering. This trend is similar to that in silicon (Si) MOSFETs, proving that the Coulombic scattering factor which originates from the high value of D_{it} is effectively minimised. On the other hand, the electron mobility of the MOSFETs having a gate dielectric grown at 1150 °C for 180 min increased with temperature. This is a clear indication that the electron mobility of such devices is limited by the Coulomb scattering which is due to the high concentration of C defects generated during the oxidation process at 1150 °C. Apart from the devices discussed above, a number of MOSFETs were also fabricated using the low

thermal budget technique but with varying temperatures and times. The channel mobility results for these devices show that, as the field effect mobility increases, the SS value decreases, proving that the interface traps also affect the subthreshold region.

Further investigation of the ultrathin SiO_2 layer was then carried out in order to reduce values of D_{it} and thus to enhance electron mobility as well as to reduce the value of ΔV_{th}. The value of ΔV_{th} needs to be as small as possible in order to control the stability of the MOSFETs. So, instead of the fabrication processes performed in chapter 4 and 5, an alternative method to form an ultrathin SiO_2 layer was introduced. In chapter 6 of this thesis, this novel method to form an ultrathin SiO_2 layer between deposited SiO_2 and 4H-SiC to complete the gate dielectric of n-type MOS capacitor was discussed. Initially, 30 or 60 nm of SiO_2 was deposited using Plasma Echanced Chemical Vapour Deposition (PECVD) followed by an annealing process at 1175 °C in N_2O gas for a variety of durations. The latter process is delibarately used to grow the ultrathin SiO_2 layer at a slow oxidation rate in order to form a uniform and high quality SiO_2 layer that generates less C defects. The deposited SiO_2 layer was used to reduce the value of ΔV_{fb}, since the SiO_2 layer has no issues regarding the charge state in the bandgap and it can also withstand a higher annealing temperature without becoming crystallized. The lowest value of D_{it} of 1.76×10^{12} $cm^{-2}eV^{-1}$ was obtained from these n-type MOS capacitors using the gate dielectric formed by 60 nm of deposited SiO_2 followed by post-oxidation annealing (POA) in N_2O ambient at 1175 °C for 90 nm. These MOS capacitors had a grown SiO_2 layer of 0.68 nm thick, as estimated using the Deal-Grove model. A ΔV_{fb} value of 0.3 V was obtained from these devices, which is much smaller than that in a gate stack consisting of Al_2O_3 as discussed in previous chapters. Measurements up to 300 °C demonstrated that the MOS capacitors with a gate stack of 60 nm SiO_2 followed by a 90 min N_2O anneal are stable at high temperature. In addition, such devices also exhibited an acceptable value of ϕ_B at 2.55 eV, which is higher than that in the gate dielectric consisting of Al_2O_3 and it can also withstand an electric field as high as 9.4 MV/cm with a leakage current density of approximately 1×10^{-3} A/cm^2.

The key objective of this thesis, which was to grow an ultrathin SiO_2 layer between the deposited dielectric and 4H-SiC using a low thermal budget technique in order to reduce the value of D_{it} and thus to enhance electron mobility in the MOSFETs, was accomplished. The insertion of an ultrathin SiO_2 layer 0.7 nm thick has effectively mitigated the issue of poor quality at the dielectric/4H-SiC interface. Further increases in thickness in this SiO_2 layer resulting from a longer duration and higher temperature of oxidation generated more C defects

and degraded the quality of the interface. However, ultrathin SiO_2 layer thicknesses less than 0.7 nm resulted in another issue of lower uniformity. This is due to the fact that a fully formed SiO_2 layer needs at least 4 Si atoms across, which corresponds to a physical thickness of approximately 0.7 nm.

7.2 Future Work

This research has obtained low values of D_{it} in MOS capacitors and high electron mobility in MOSFETs by utilising a gate stack which consists of an ultrathin SiO_2 layer between the Al_2O_3 and 4H-SiC. However, these devices are still haunted by the problem of large ΔV_{th} values due to the nature of Al_2O_3, even though an optimized densification PMA has been carried out. To solve this problem, an ultrathin SiO_2 layer was grown underneath the deposited SiO_2 via POA annealing in N_2O ambient. N-type MOS capacitors were fabricated which showed the lowest values in D_{it} with a grown 0.7 nm of SiO_2 layer. By using this technique and varying the oxidation parameters, MOSFETs can be fabricated and electrical characterisation performed to determine channel mobility and current carrying capability as well as the value of ΔV_{th}.

A further investigation of MOS devices fabricated using both techniques can also be carried out. The concentration of C defects, which are believed to be the main source of high values of D_{it} which degrade channel mobility, can be observe using Time-of-Flight Secondary Ion Mass Spectrometry (ToF-SIMS). By using this characterization technique, the concentration and location of C defects can be found and further confirm electrical measurement results. Other than that, fabricated MOS devices can also be analyzed using a Scanning Capacitance Microscopy (SCM) probe to observe electrically active defect at the channel of MOSFETs. Further device characterisation will also can be performed including the device modelling, e.g. TCAD (Technology Computer-Aided Design) and device reliability, e.g. TDDB (Time Dependent Dielectric Breakdown) and BTI (Bias Temperature Instability) measurements. In order to demonstrate that the fabricated devices are suitable to be produced in large scale for commercialization, appropriate statistical analysis is required in the future. After all the aforementioned issues have been solved, the best oxidation parameters will be used to fabricate power electronic devices that require a good dielectric/4H-SiC interface, such as DMOSFET or IGBT.

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